

FIG. 1A

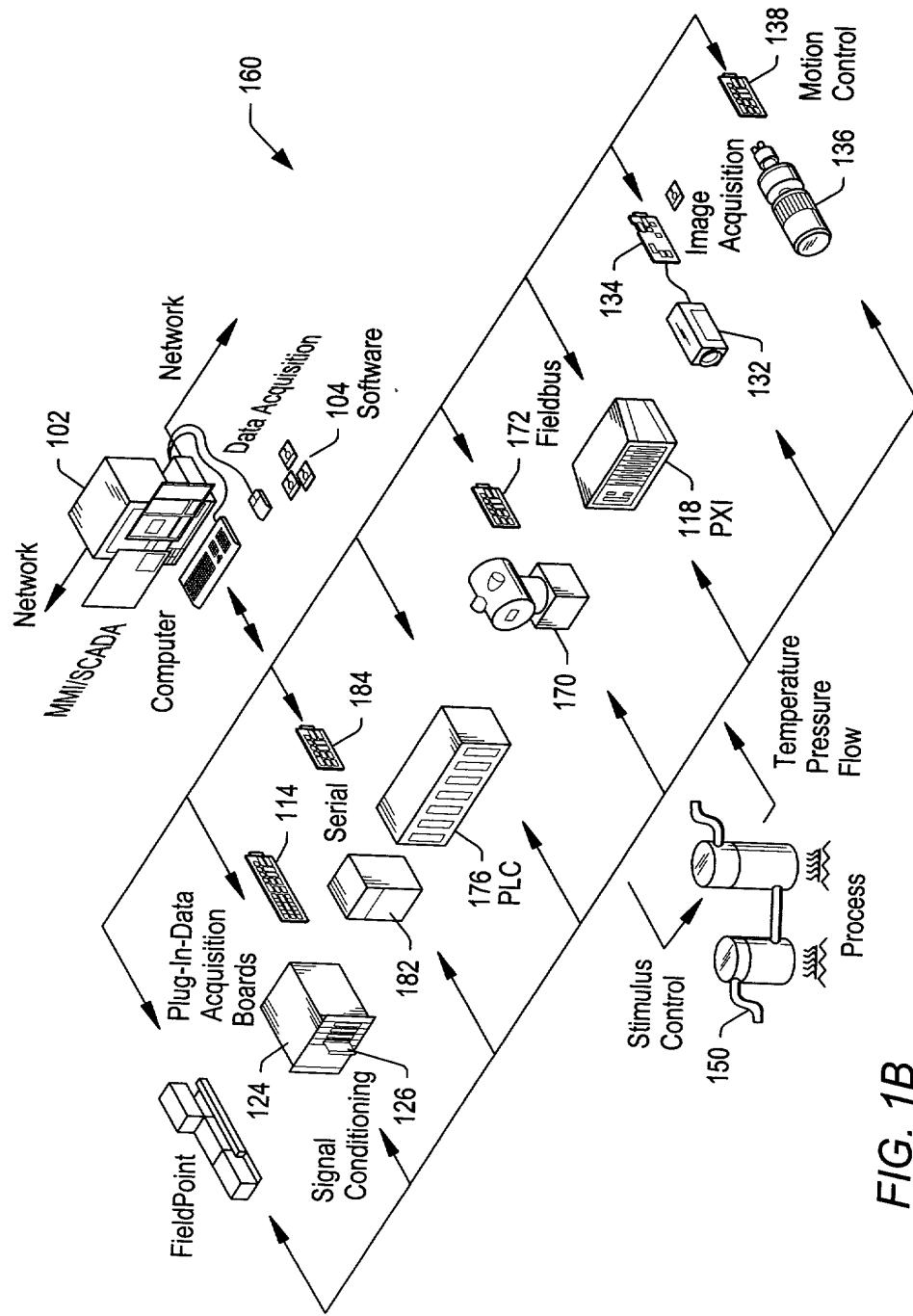


FIG. 1B

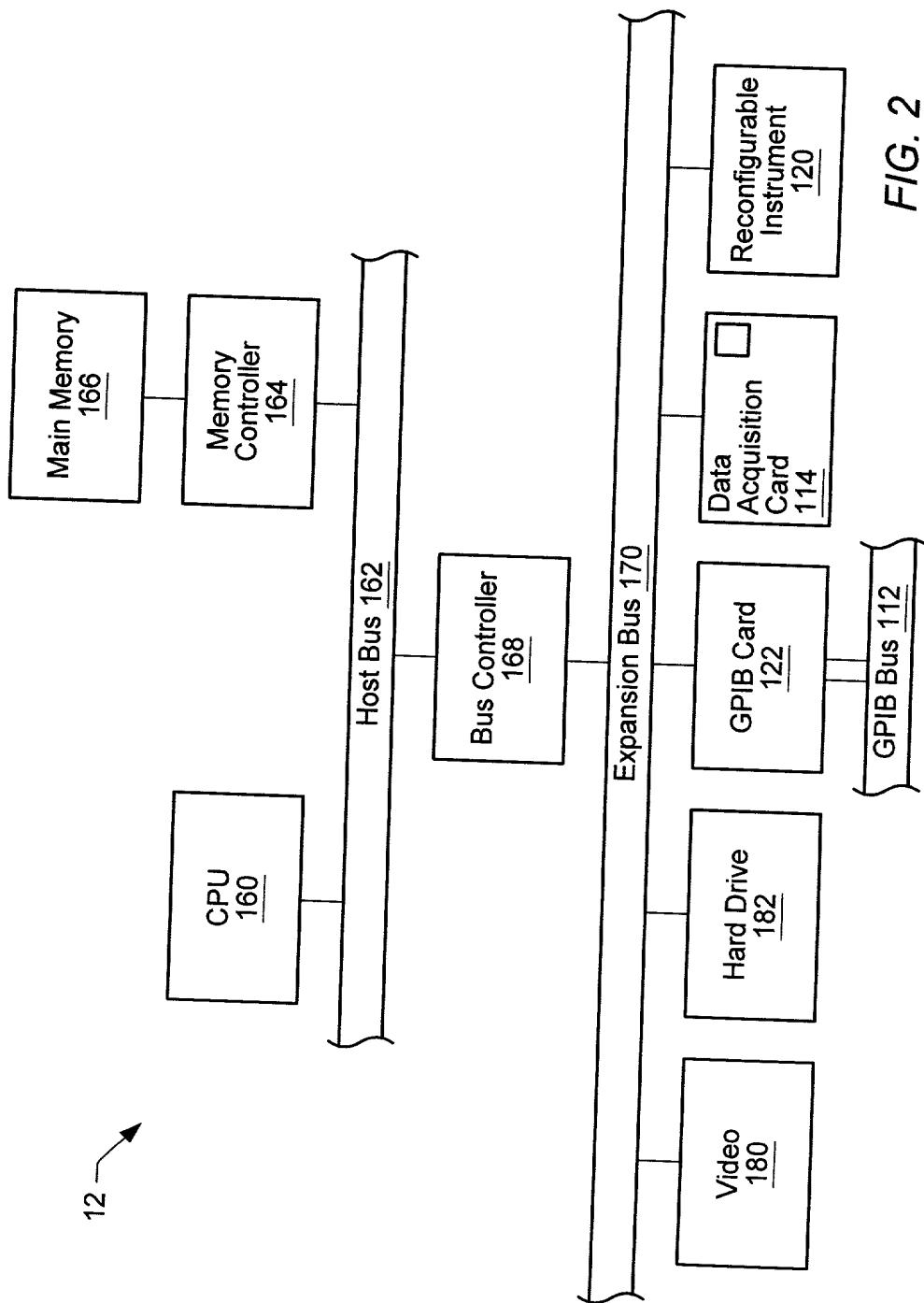


FIG. 2

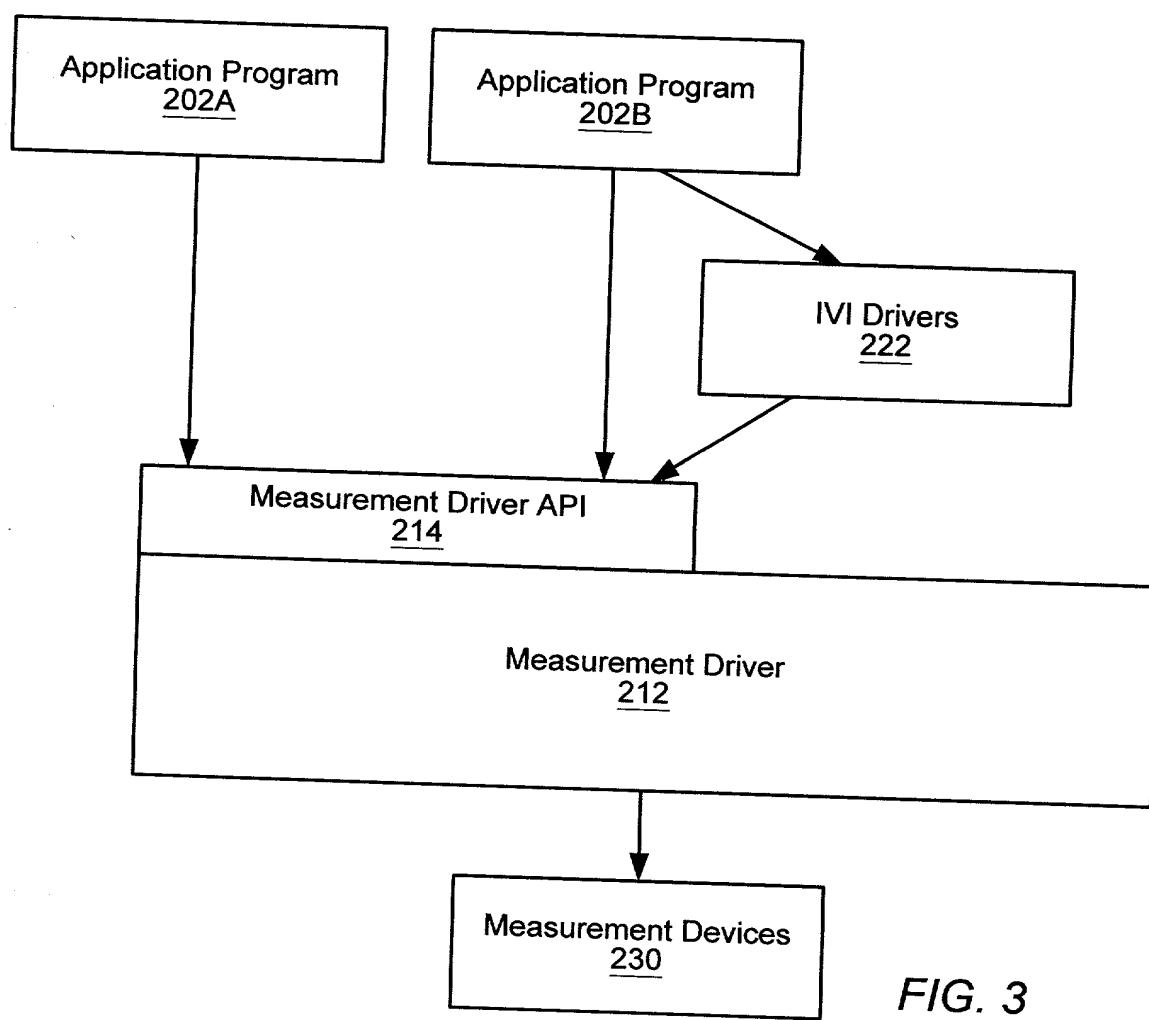


FIG. 3

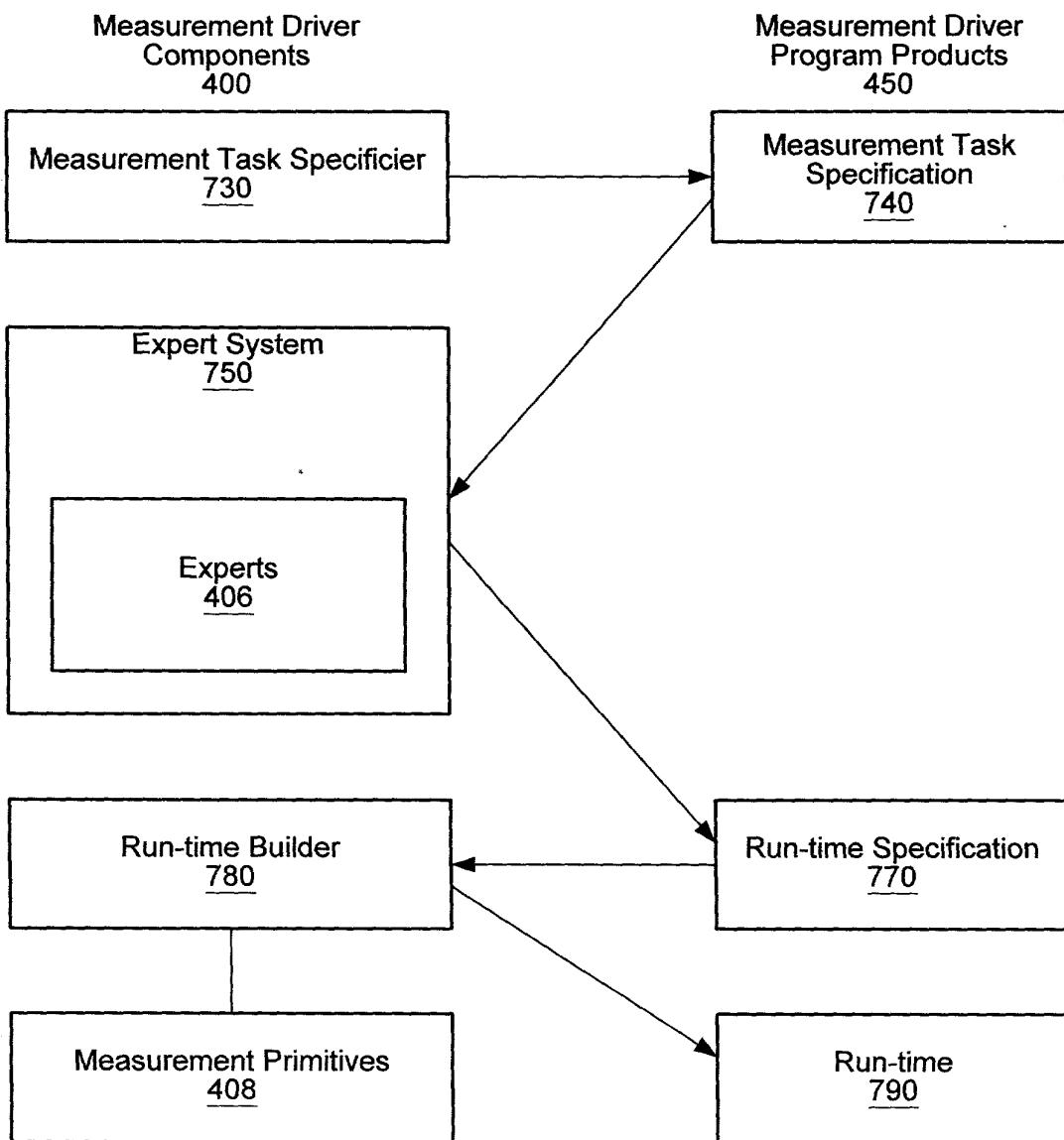


FIG. 4

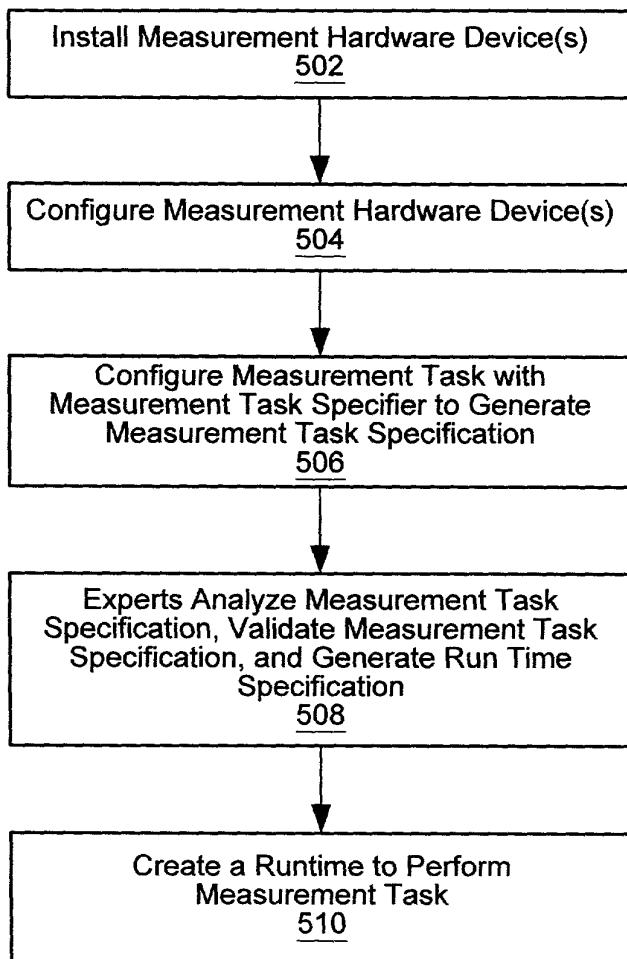
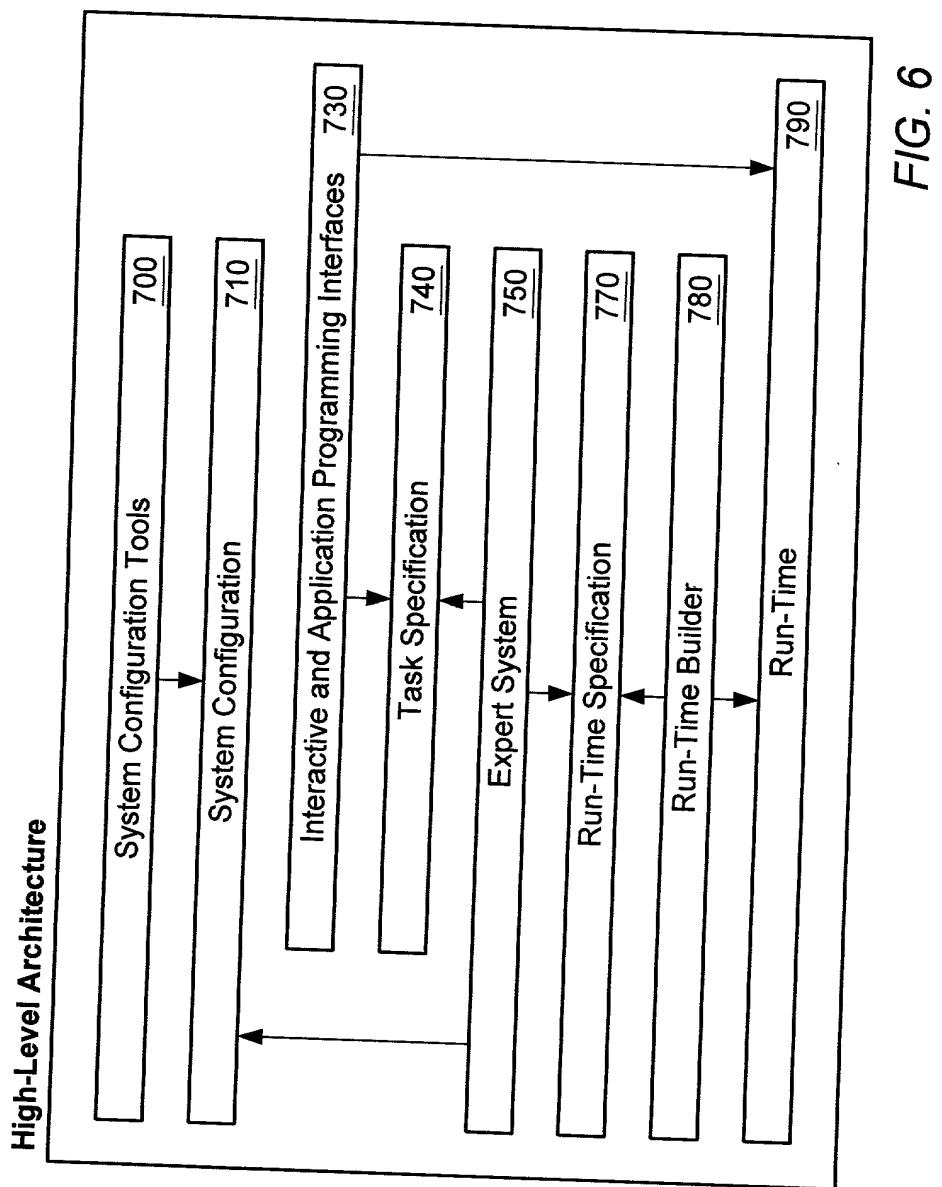


FIG. 5



System Configuration and Task Specification

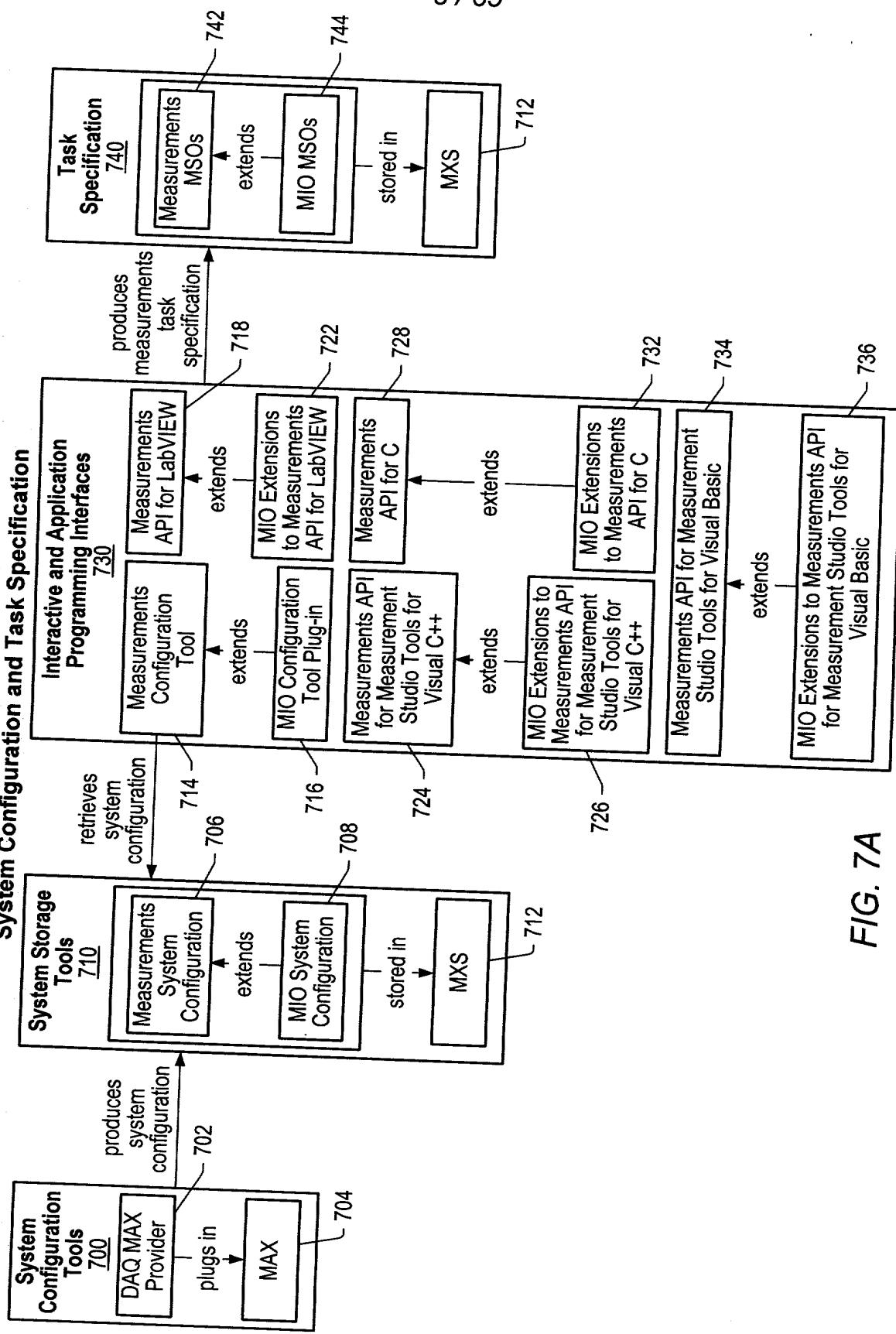


FIG. 7A

Compiling Task Specification to Task Run-time Specification

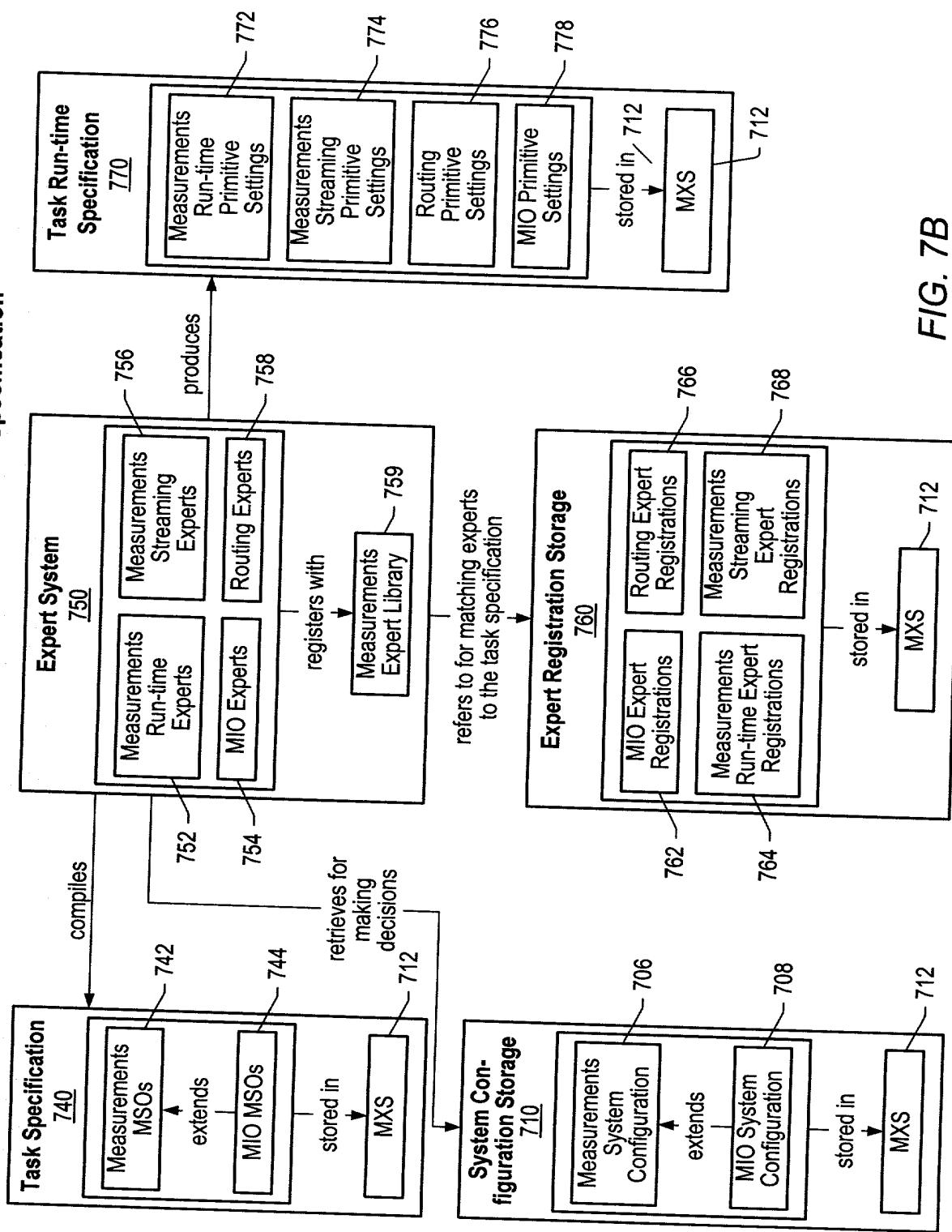


FIG. 7B

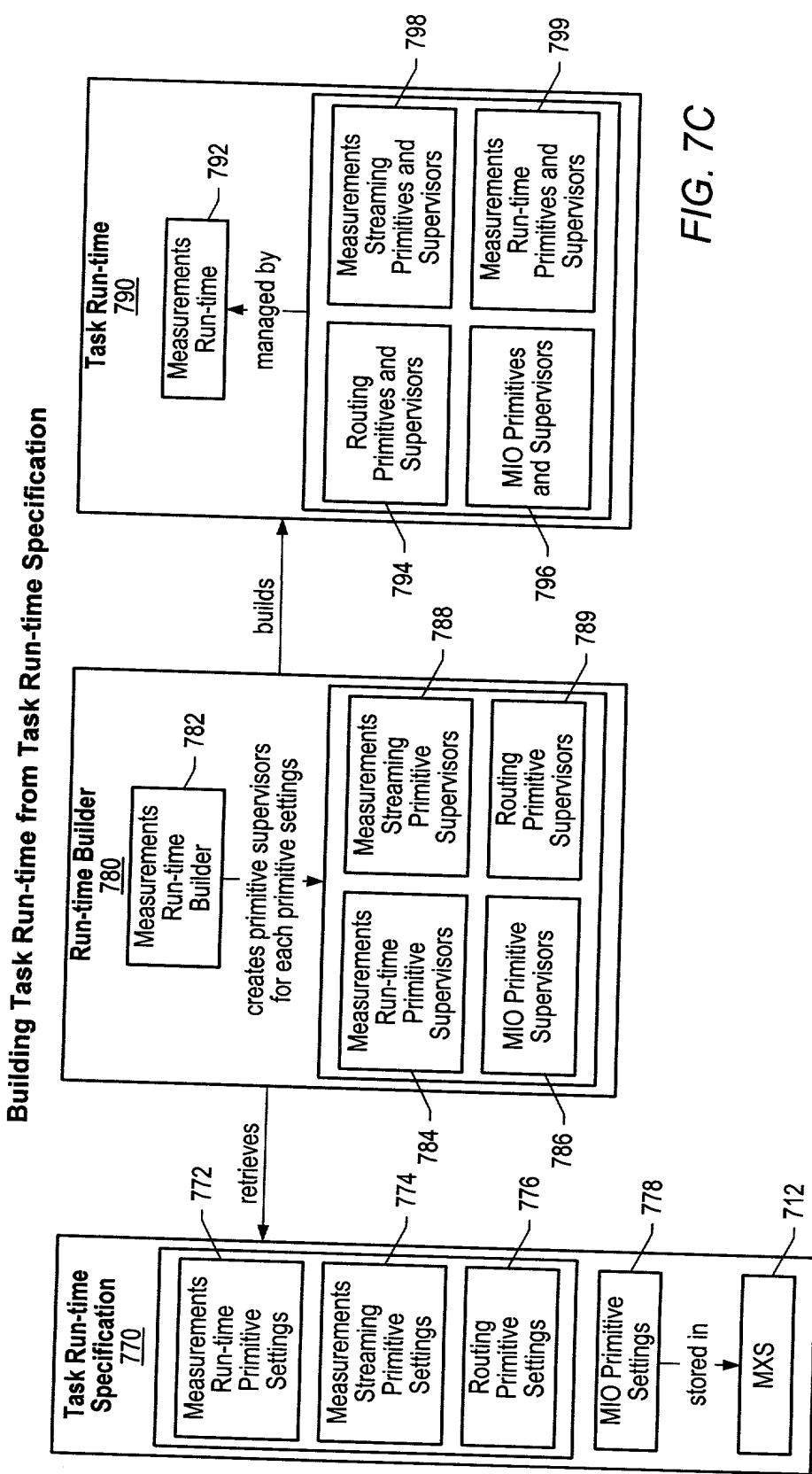


FIG. 7C

Executing Tasks

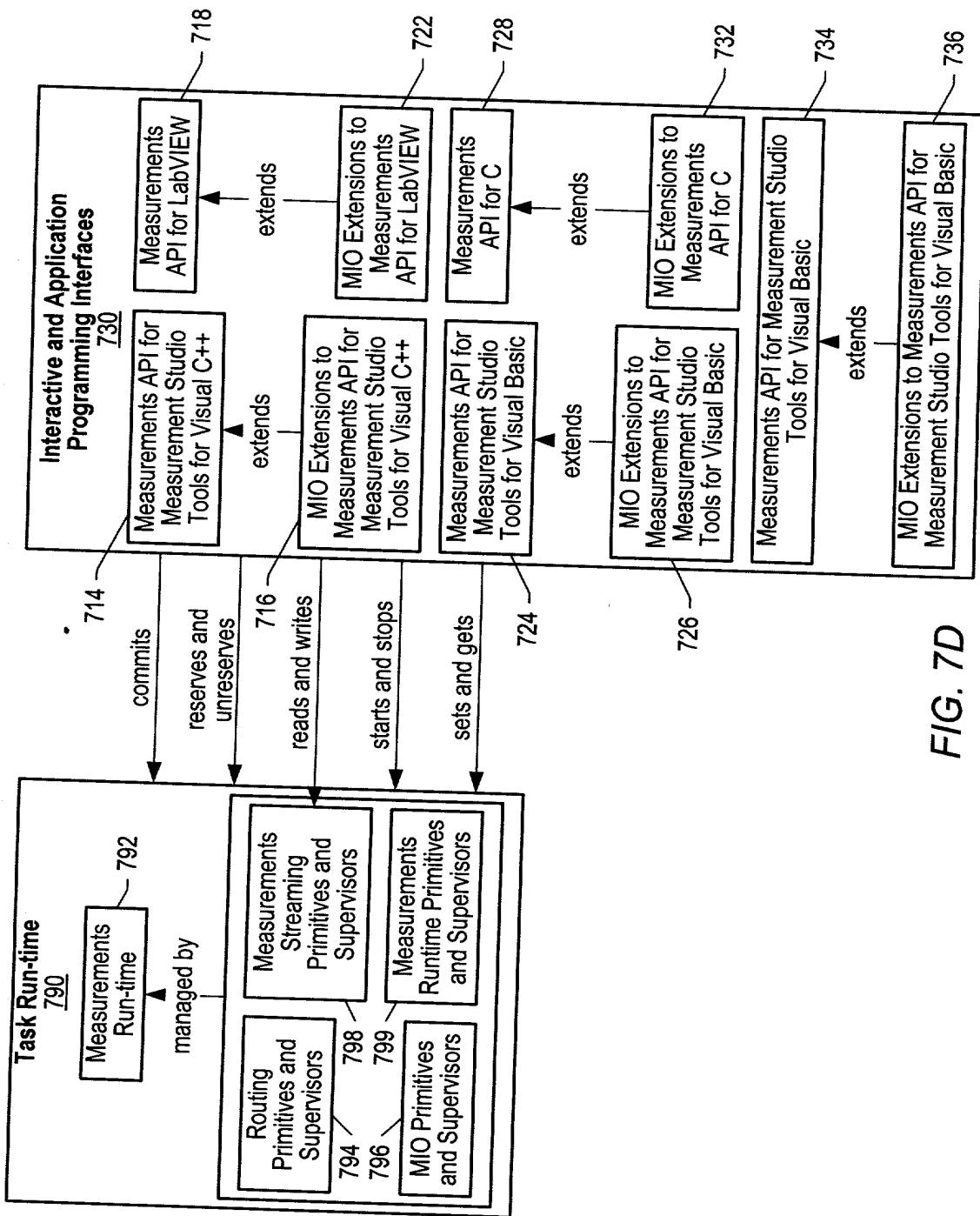


FIG. 7D

Packages for System Configuration and Task Specification

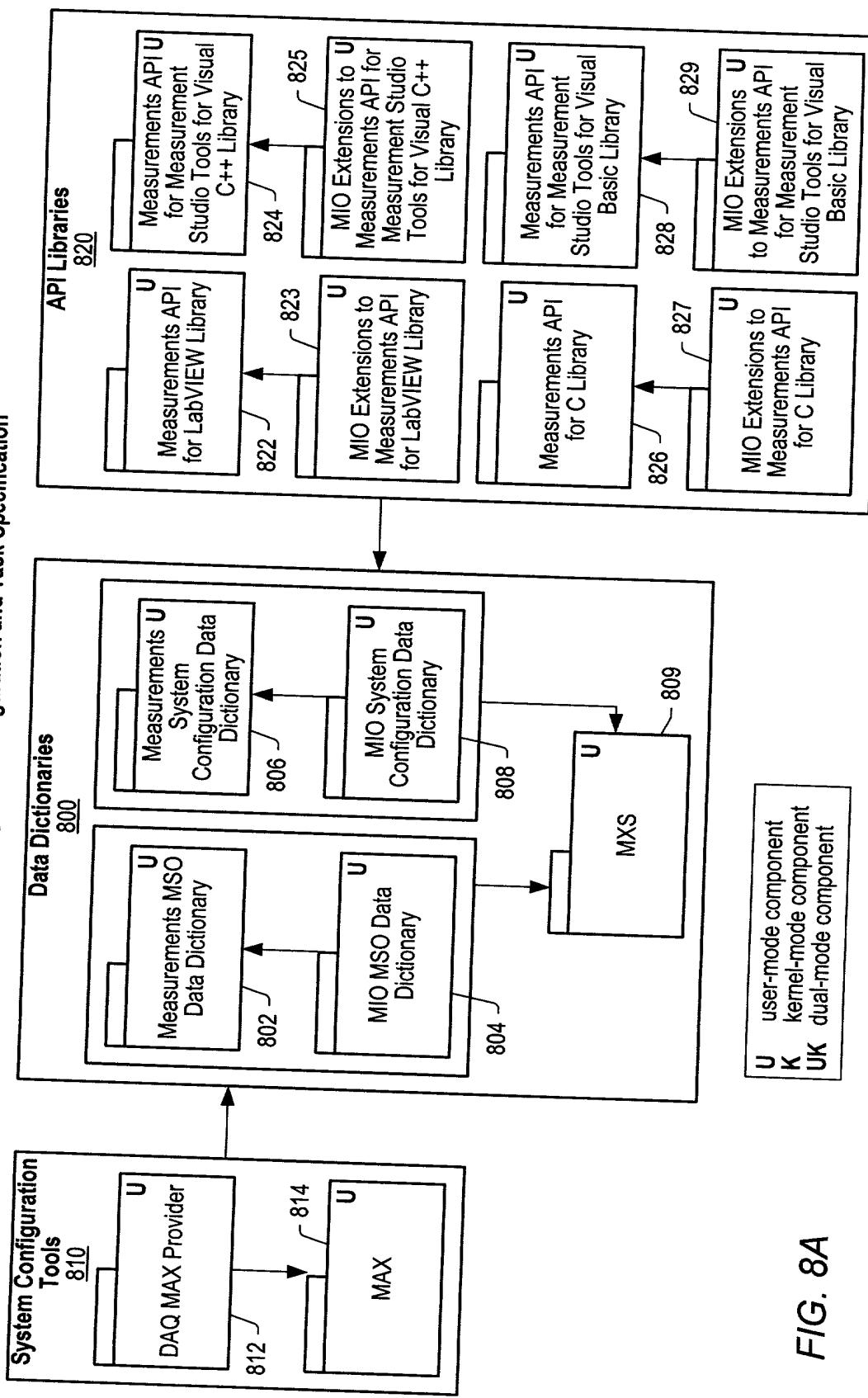


FIG. 8A

Packages for Compiling Task Specification to Run-time Specification

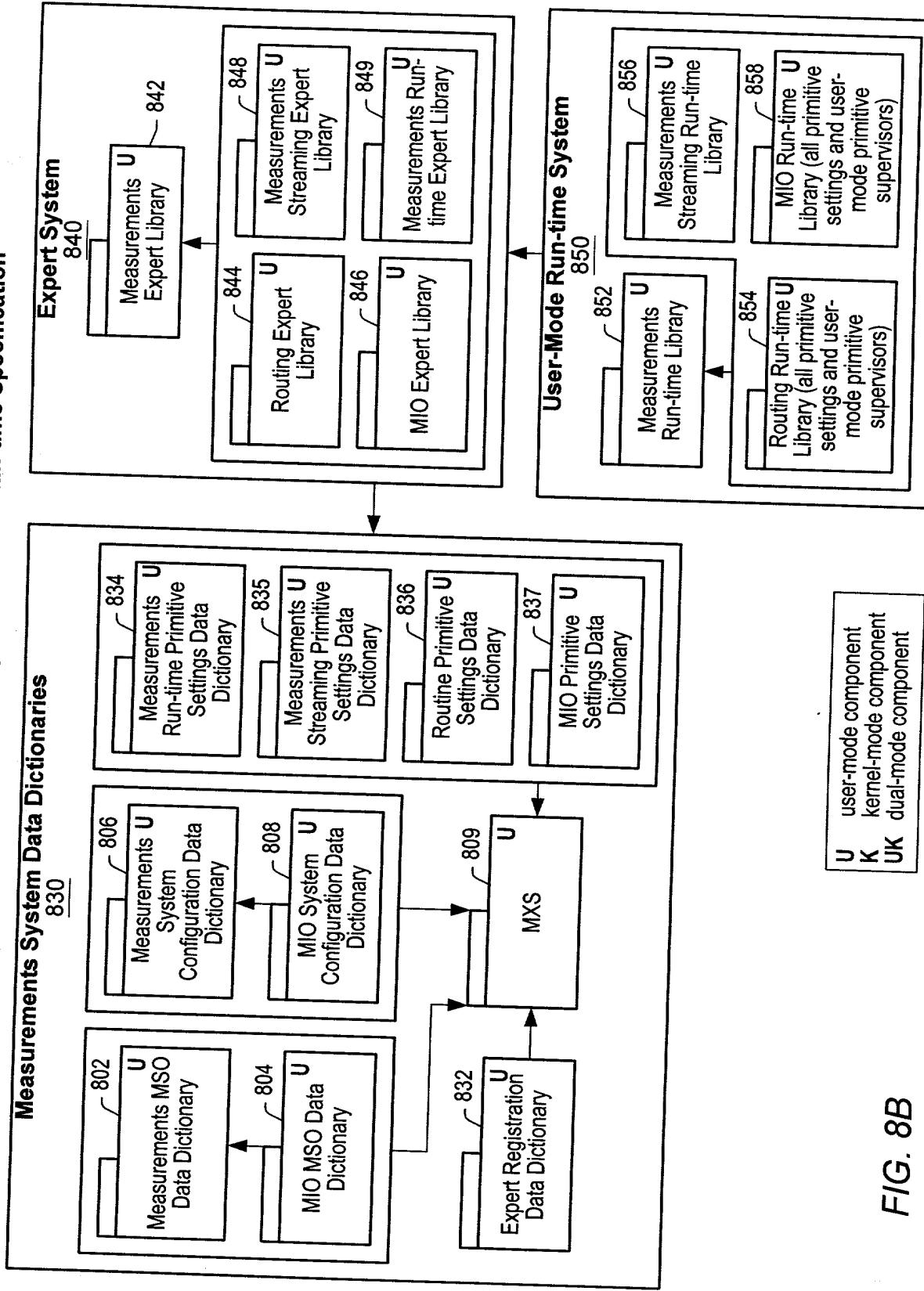


FIG. 8B

Packages for Building Task Run-time from Run-time Specification

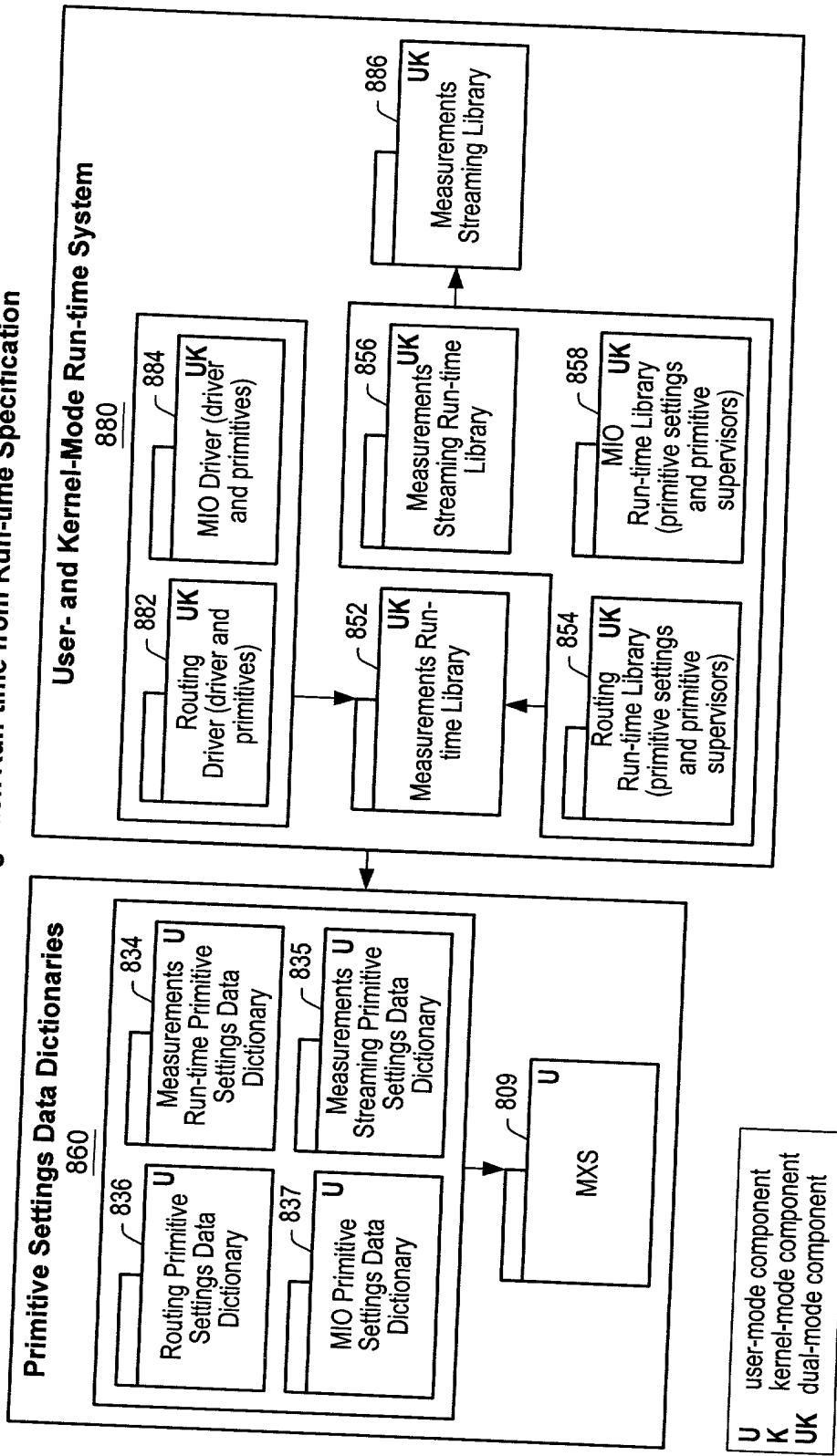


FIG. 8C

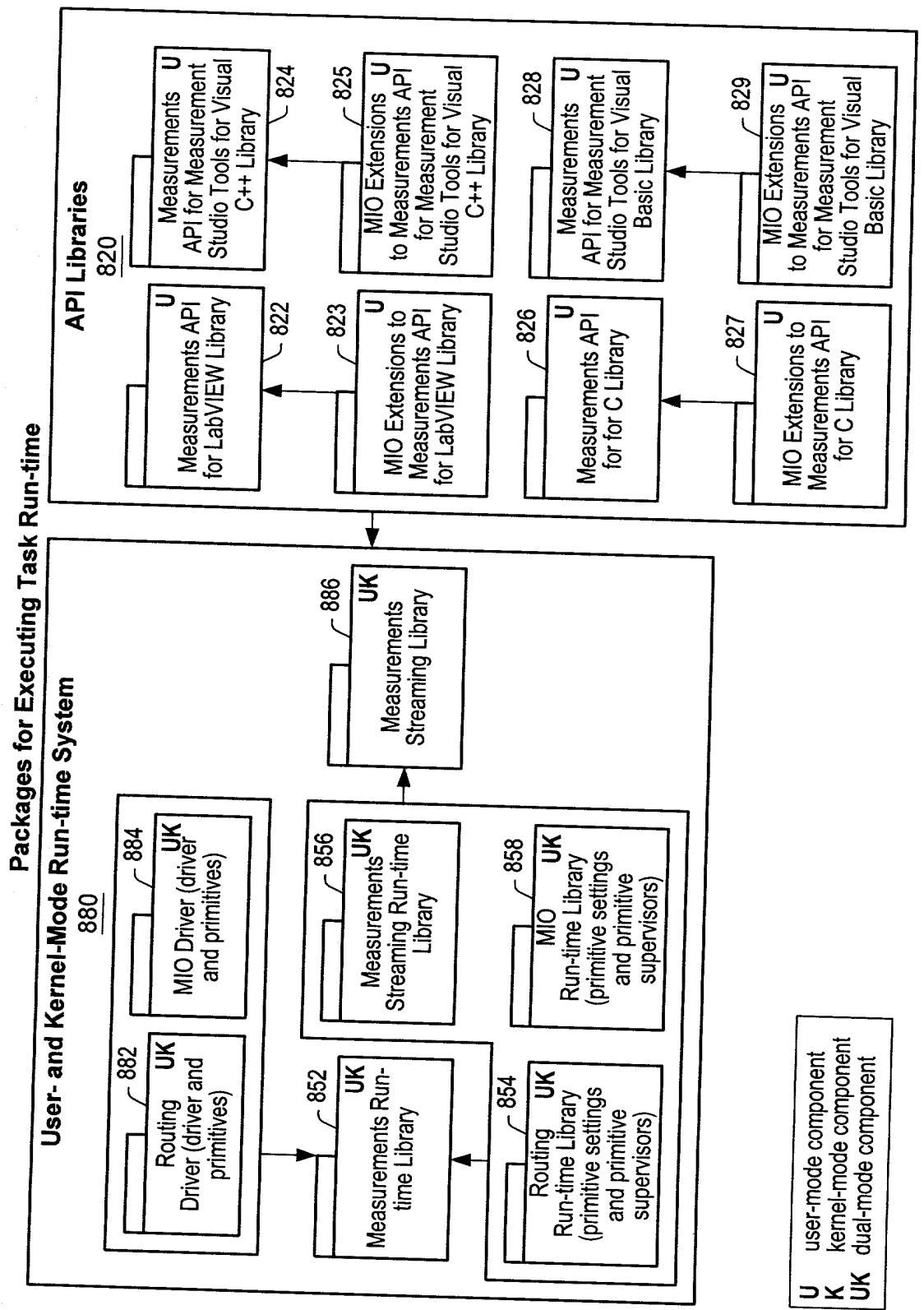
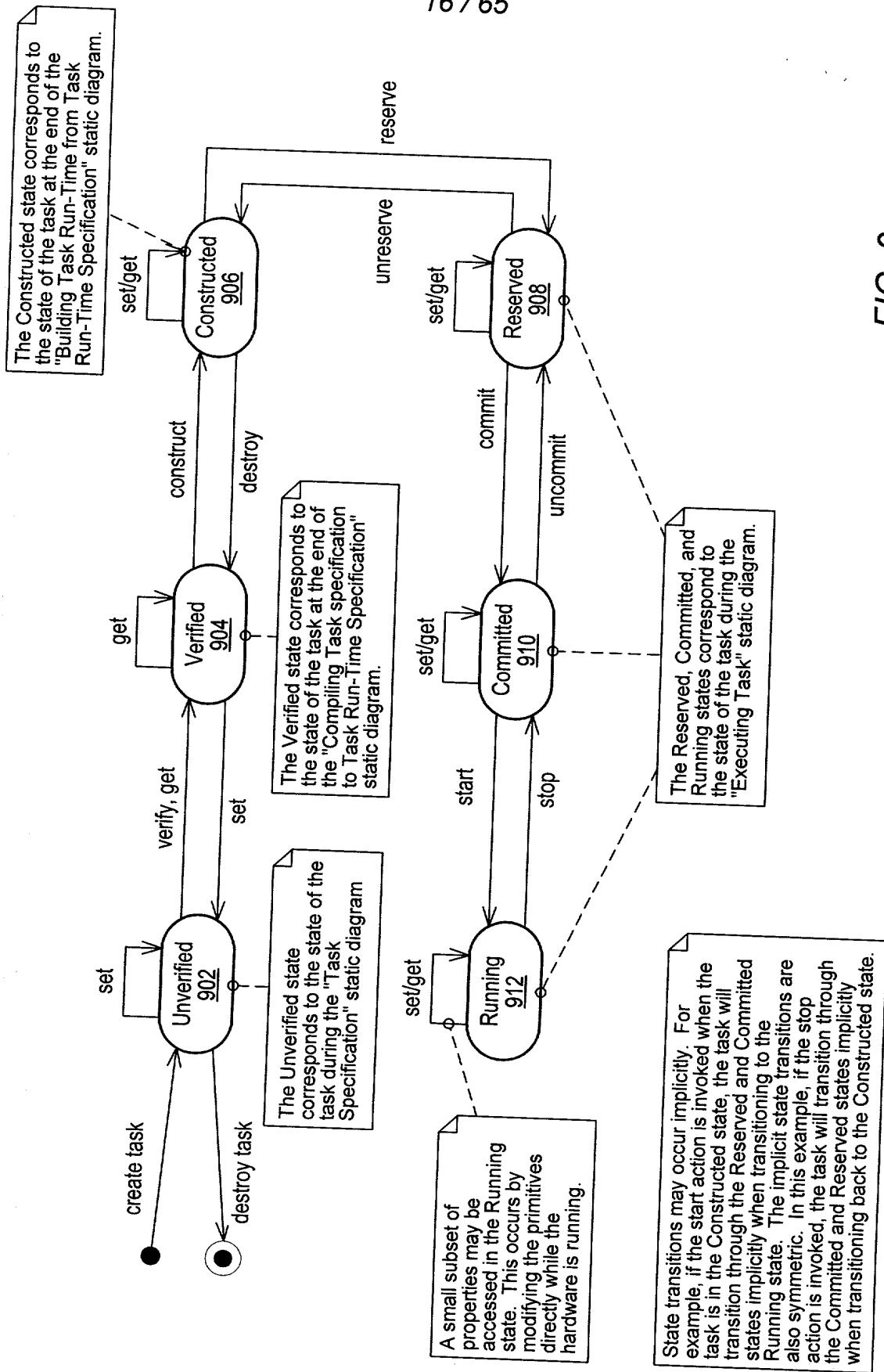


FIG. 8D

State Diagram for Measurement Tasks



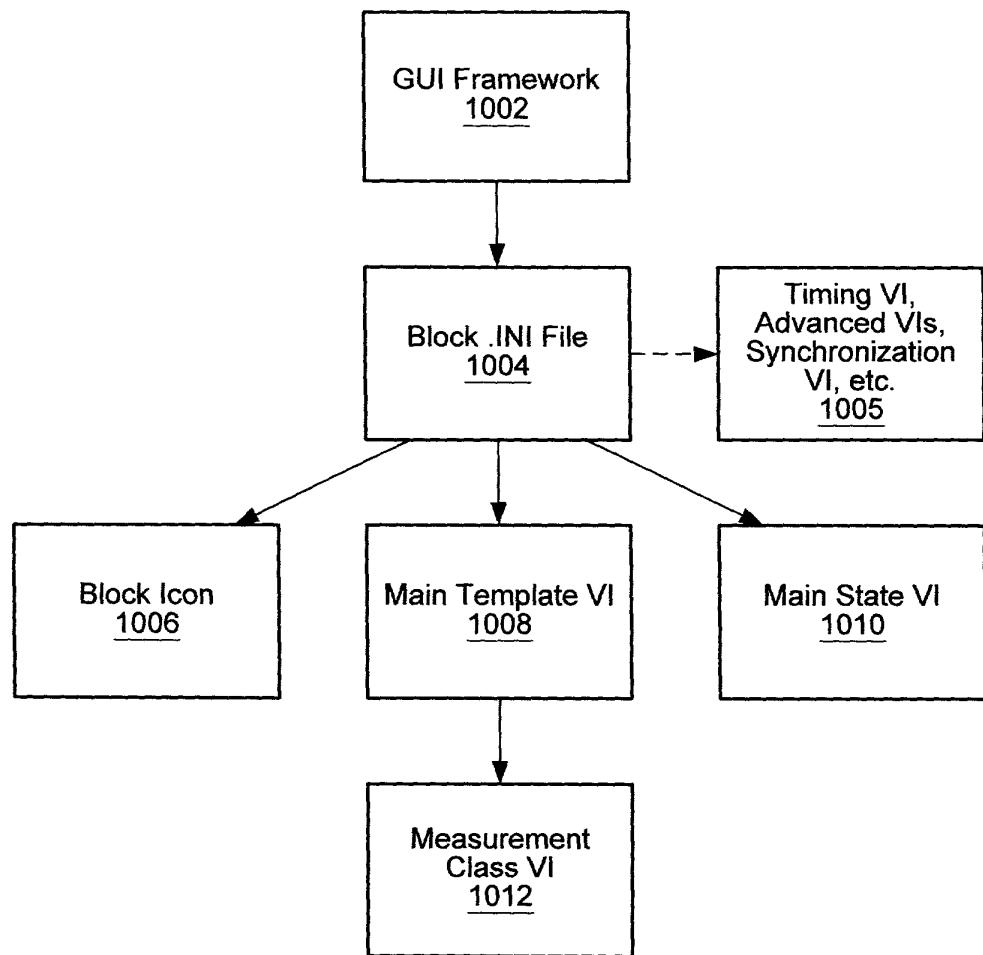


FIG. 10

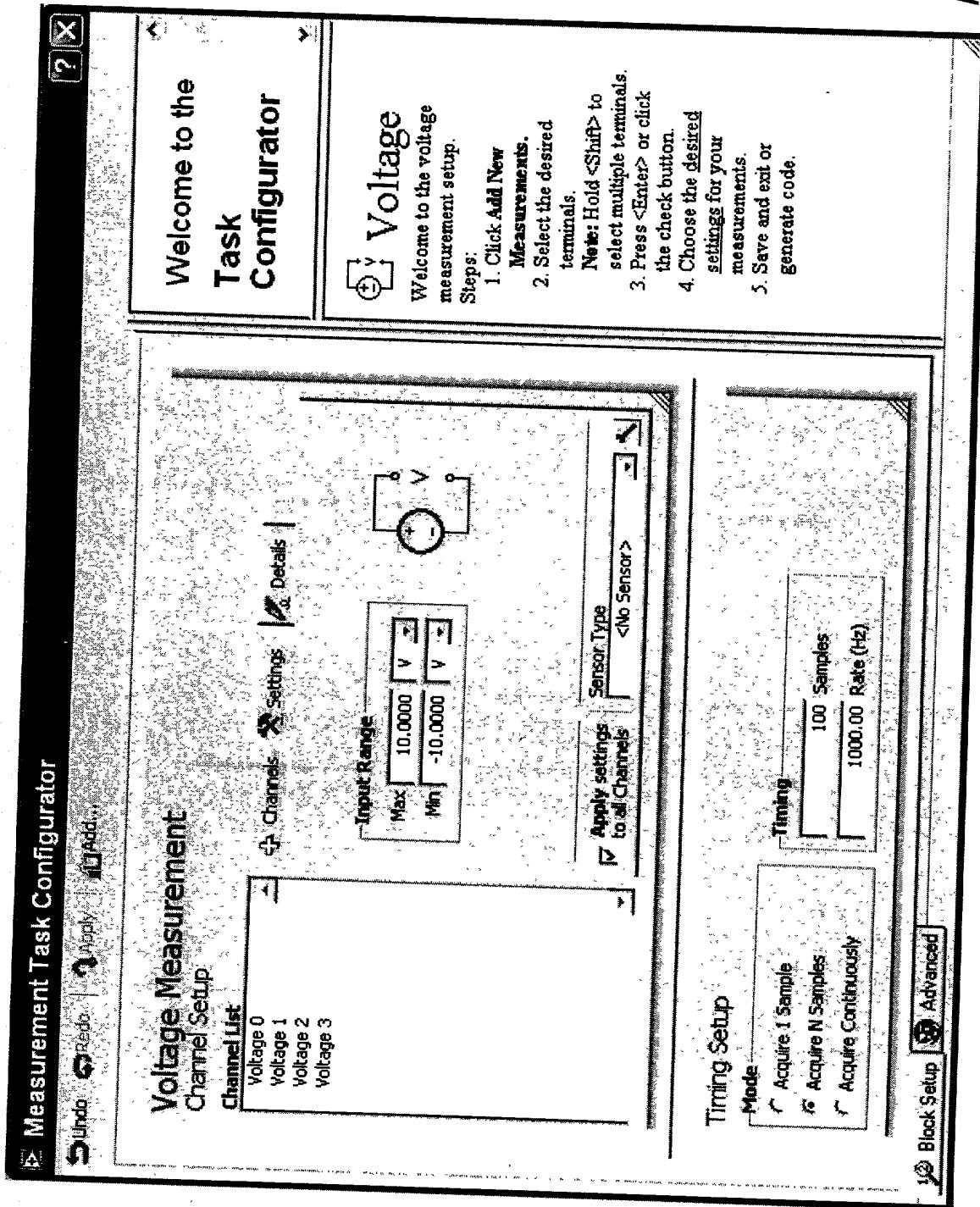


FIG. 11

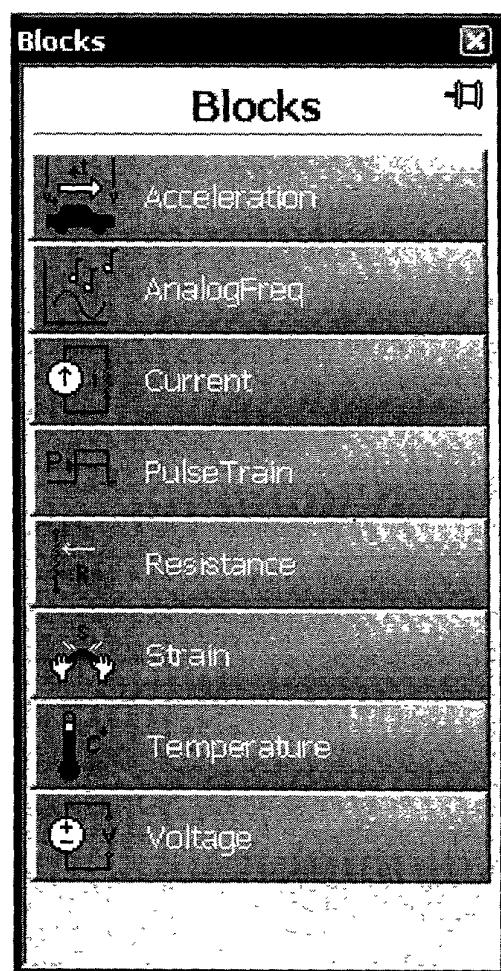
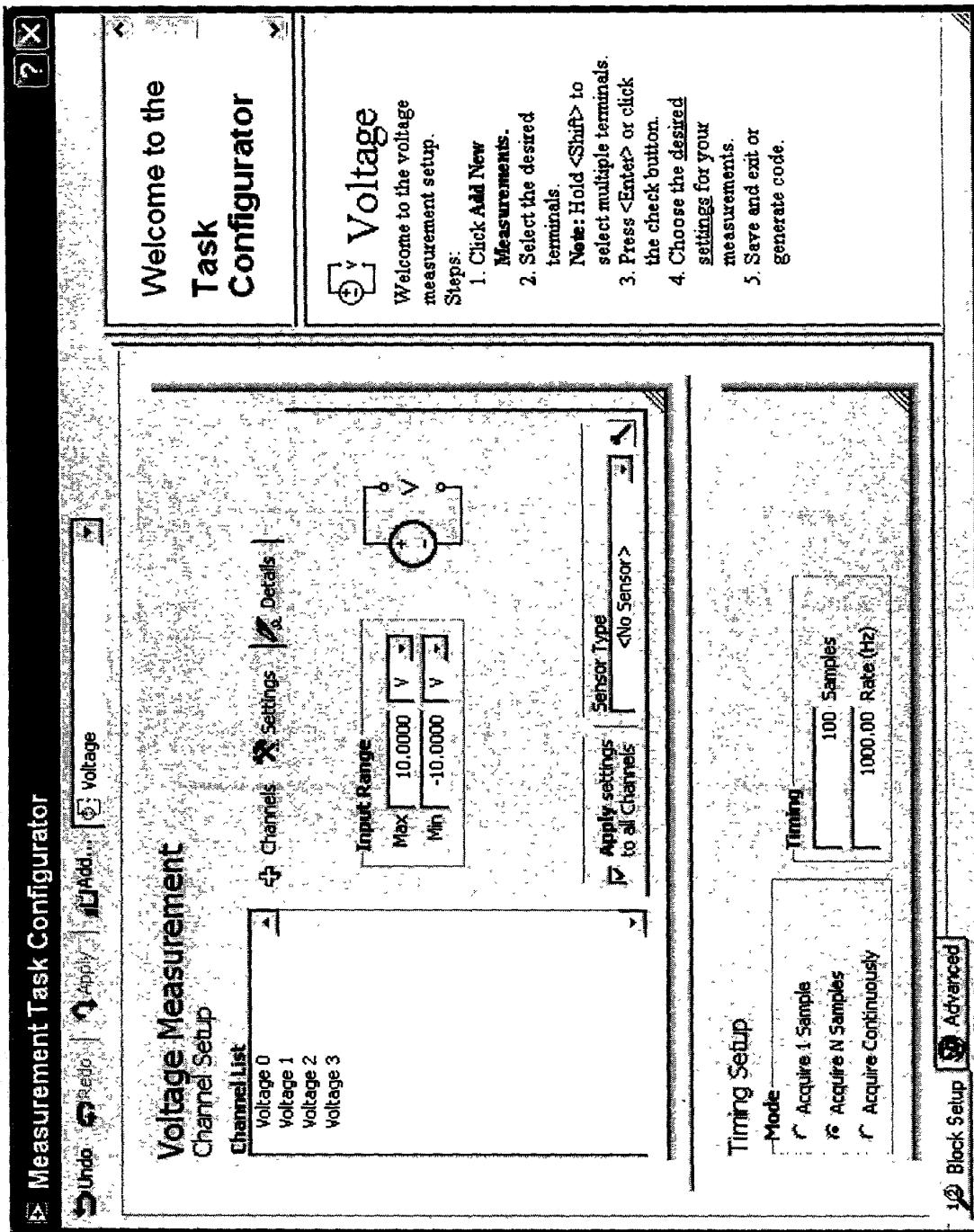


FIG. 12A

FIG. 12B



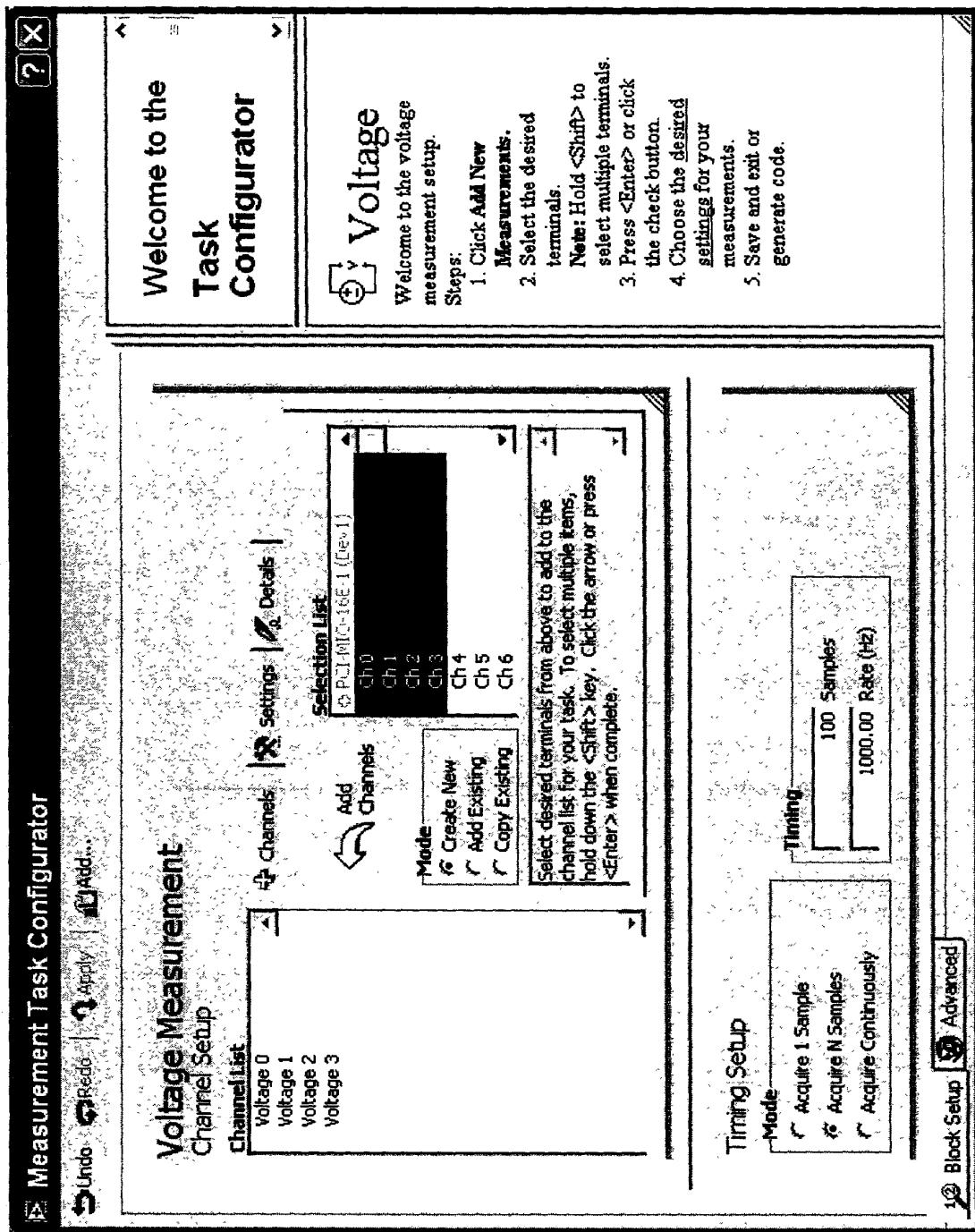


FIG. 12C

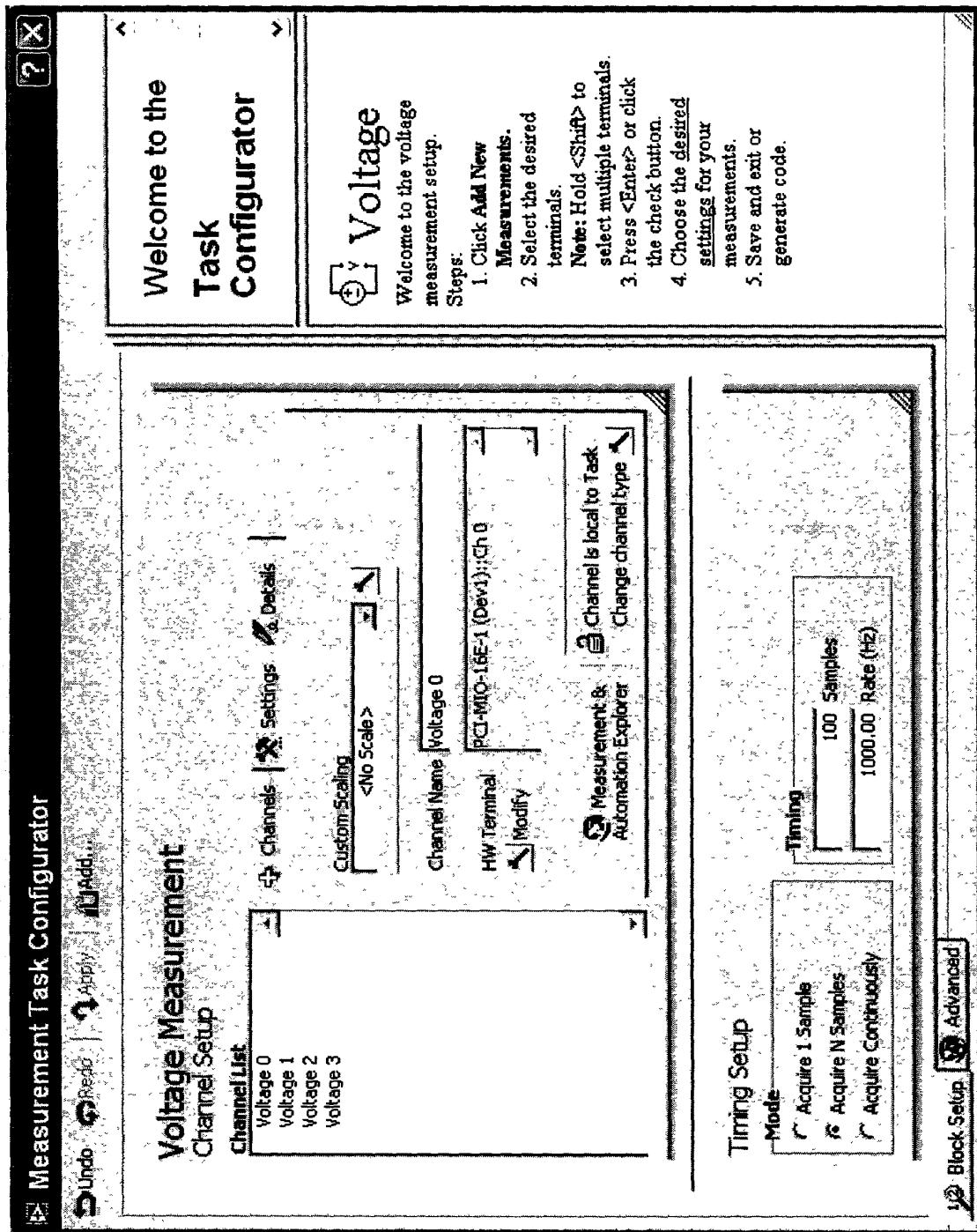


FIG. 12D

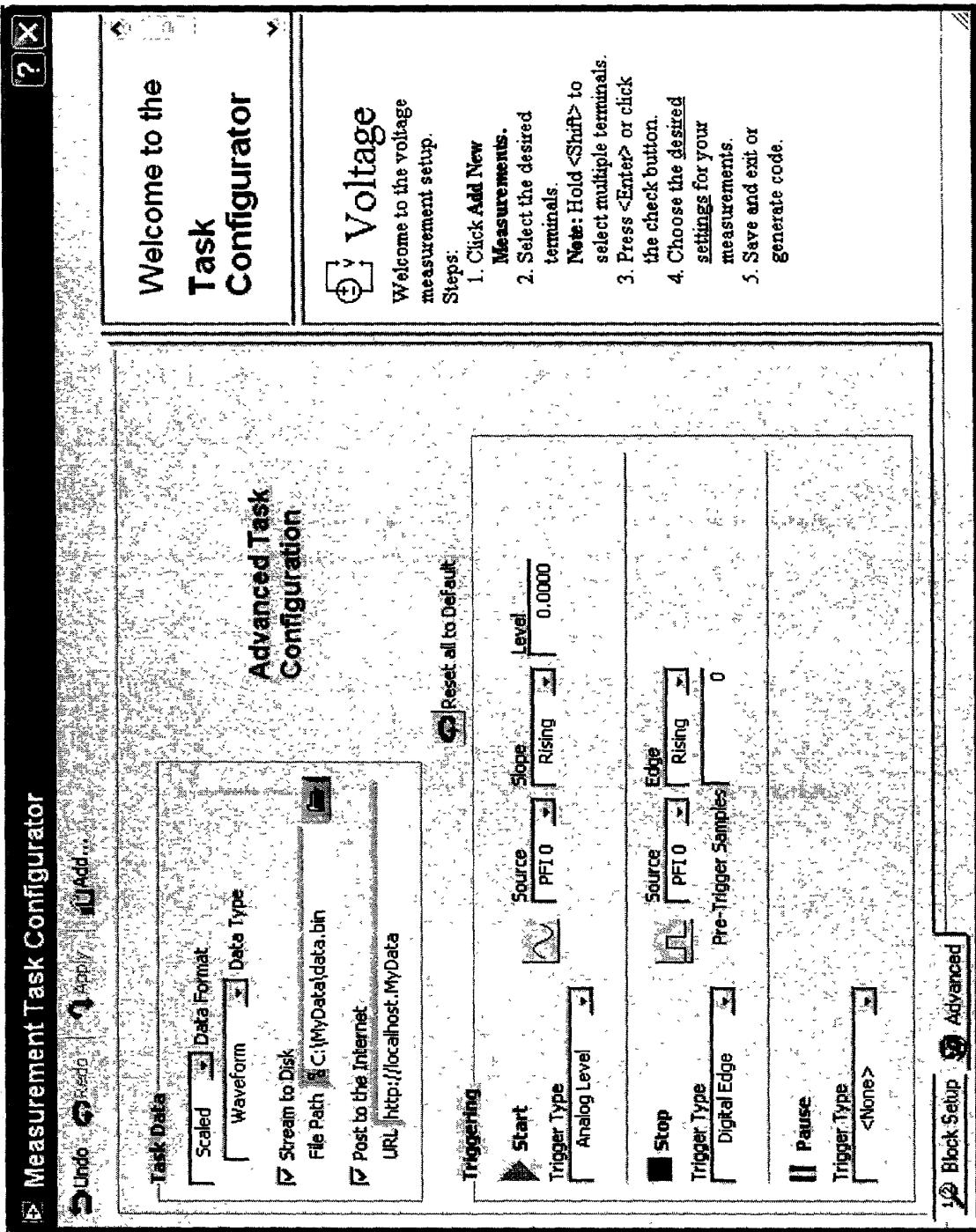
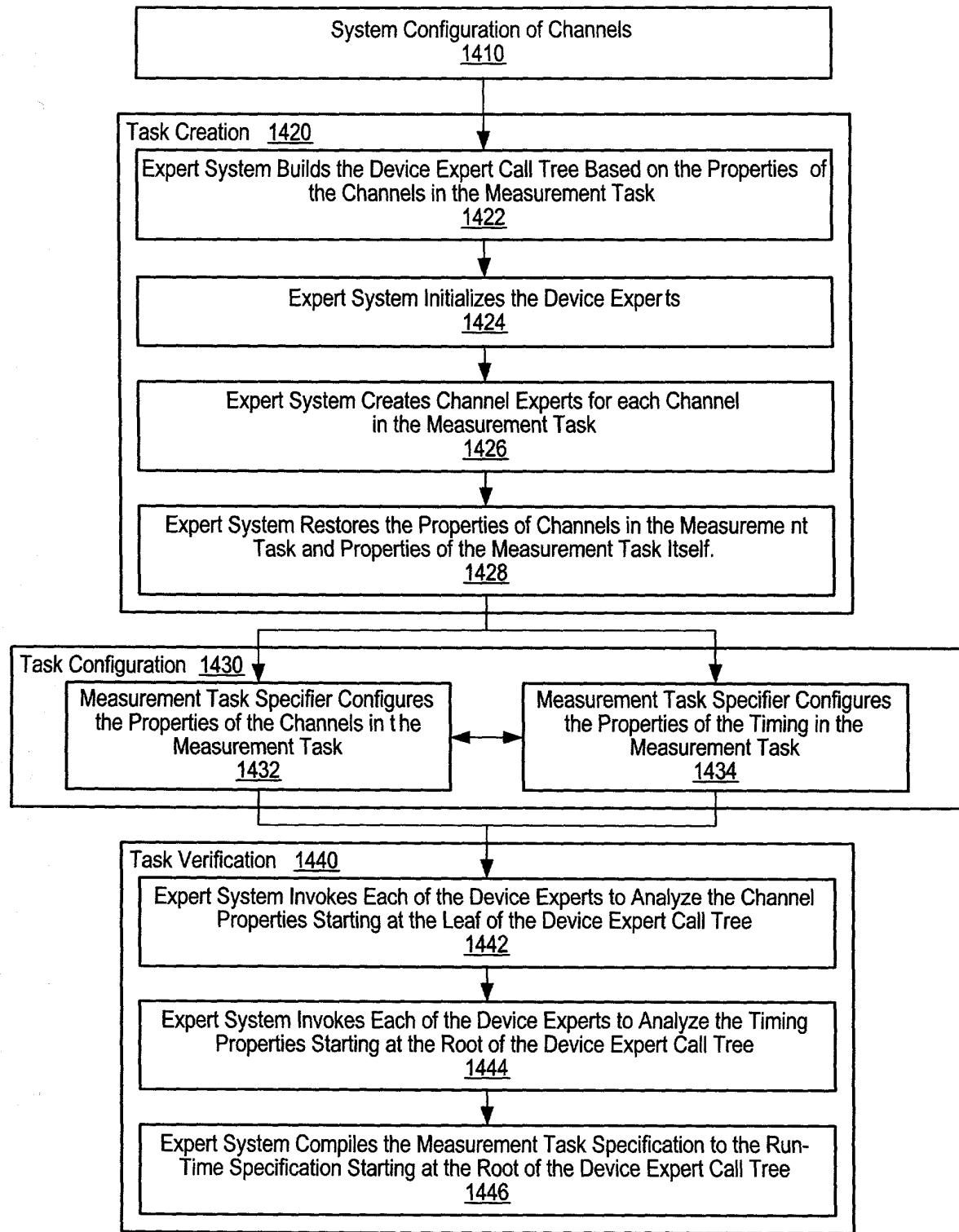


FIG. 13

**FIG. 14**

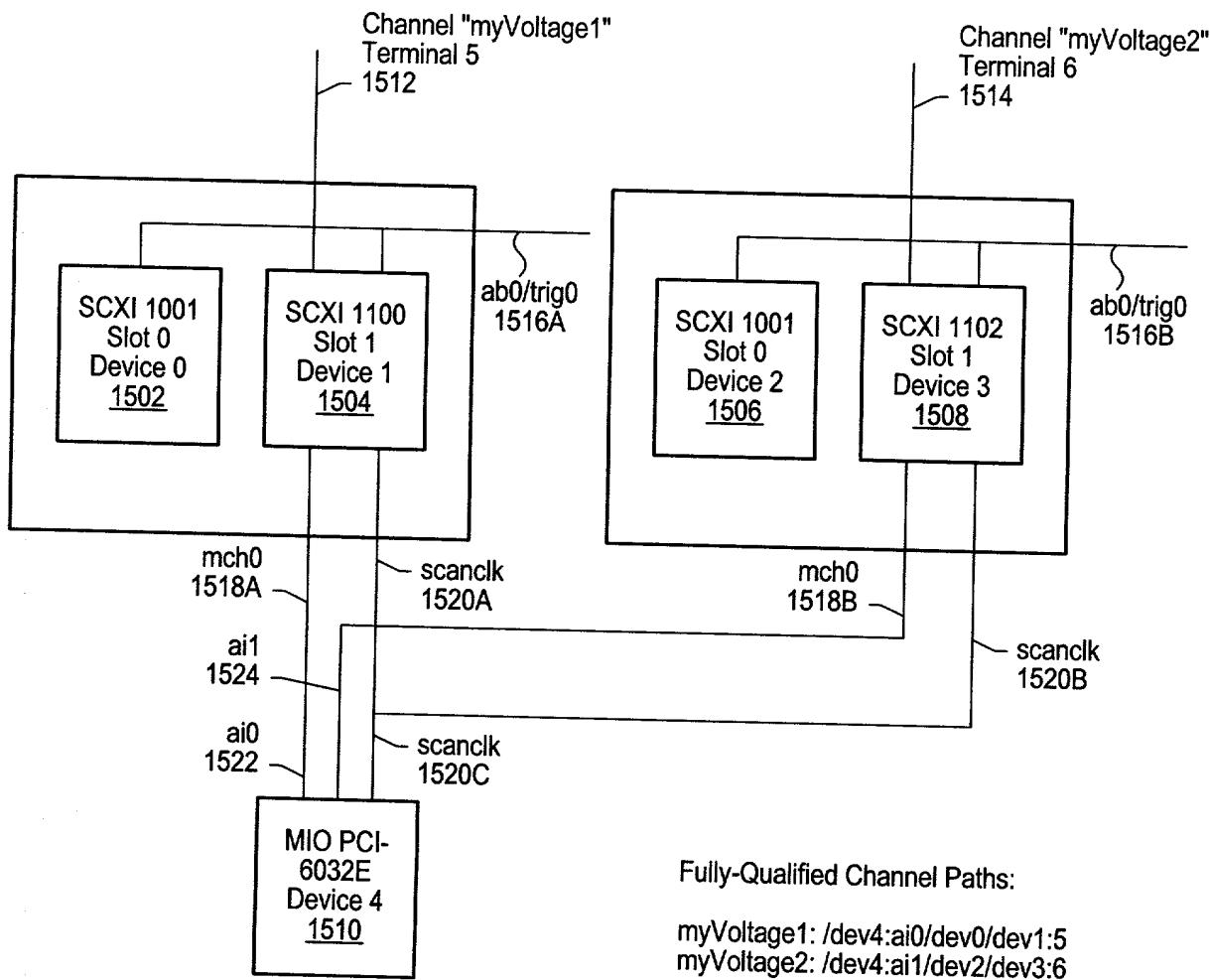
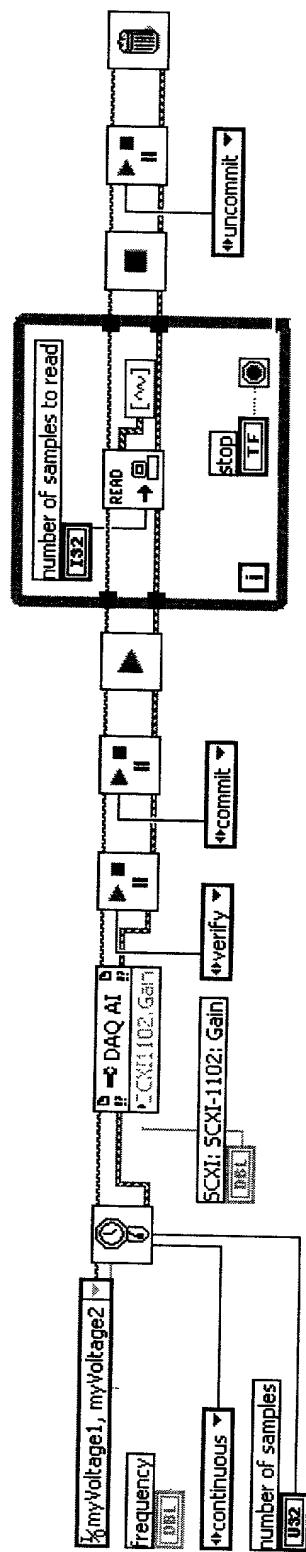


FIG. 15



Voltage On Two Channels with Two SCXI Modules in Two
SCXI Chassis Connected to an MIO DAQ Device

F/G. 16

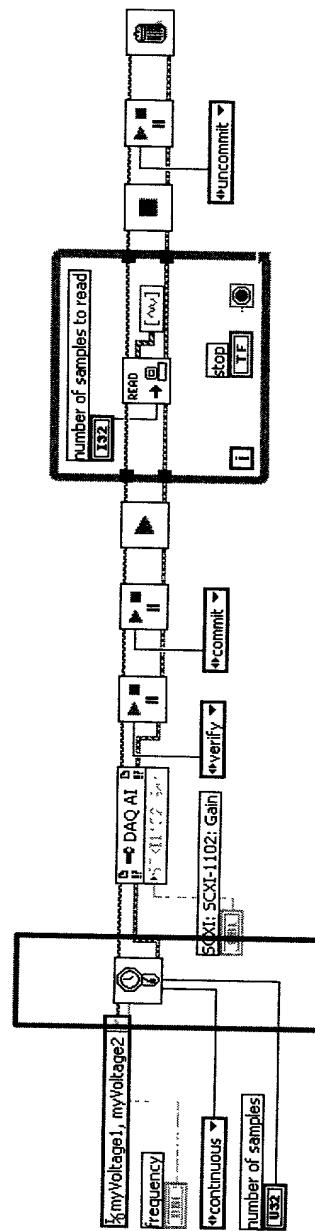
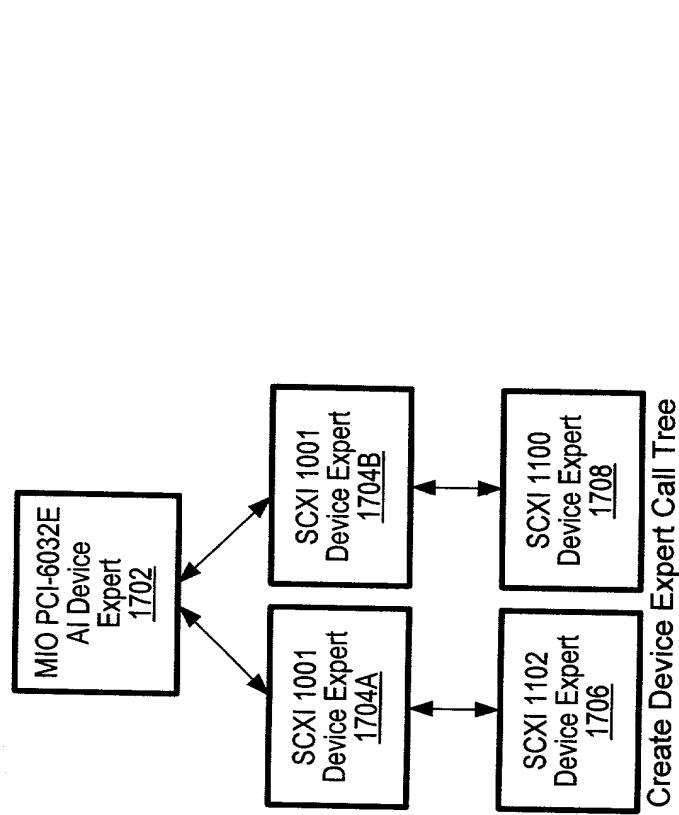


FIG. 17

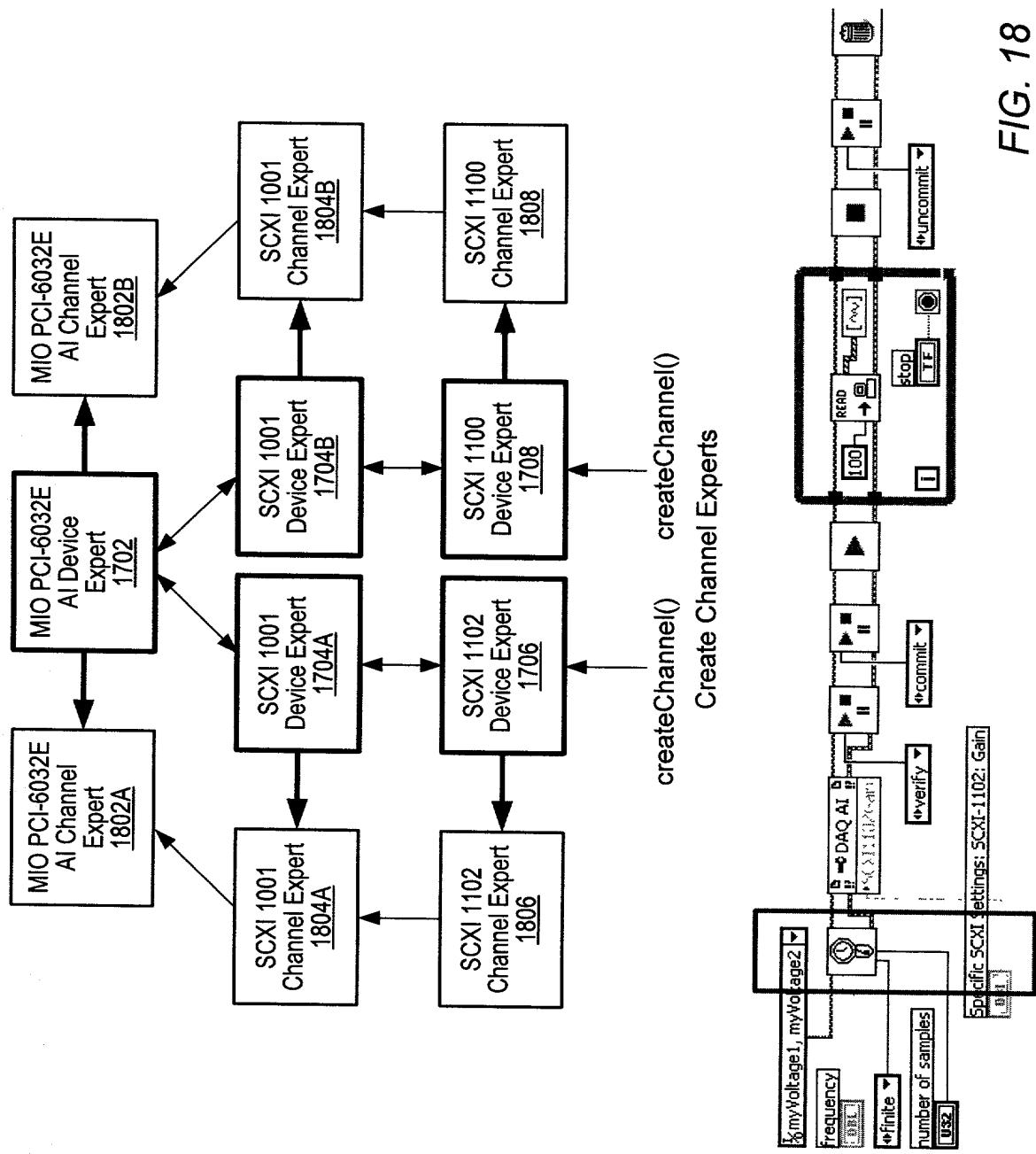
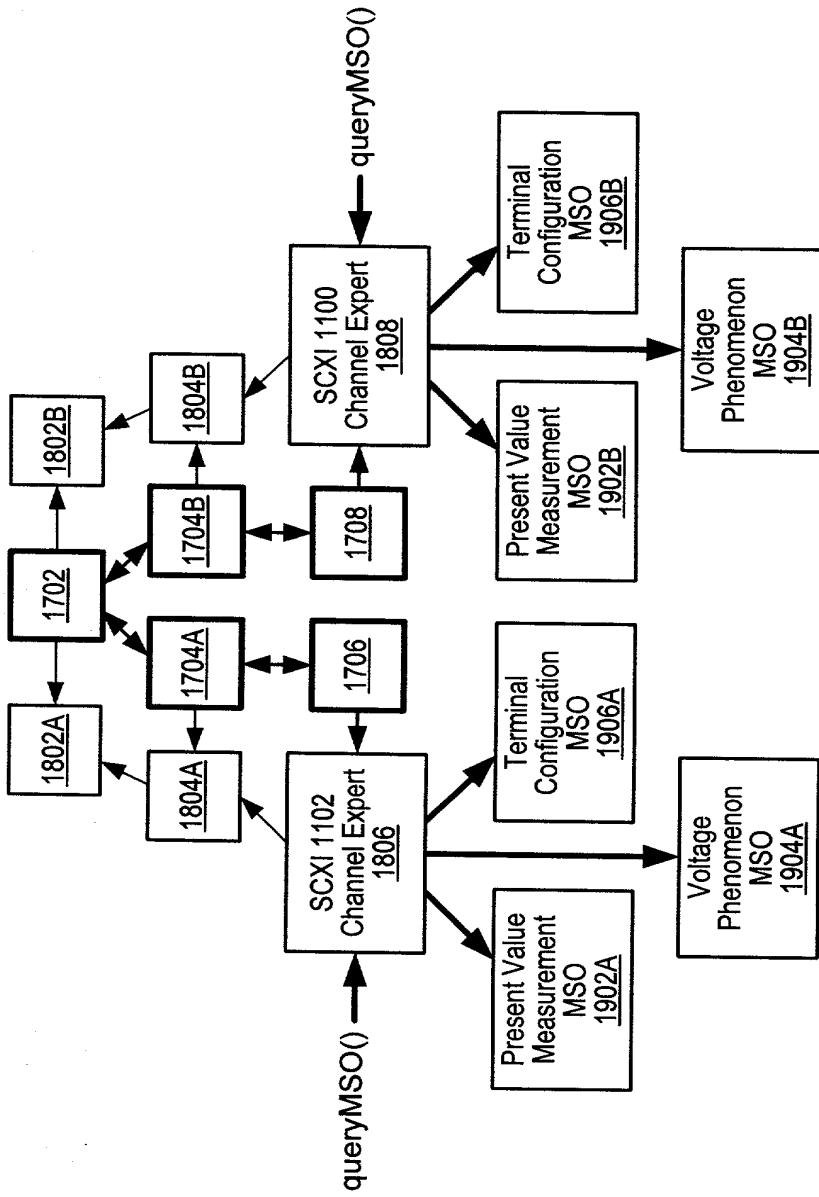
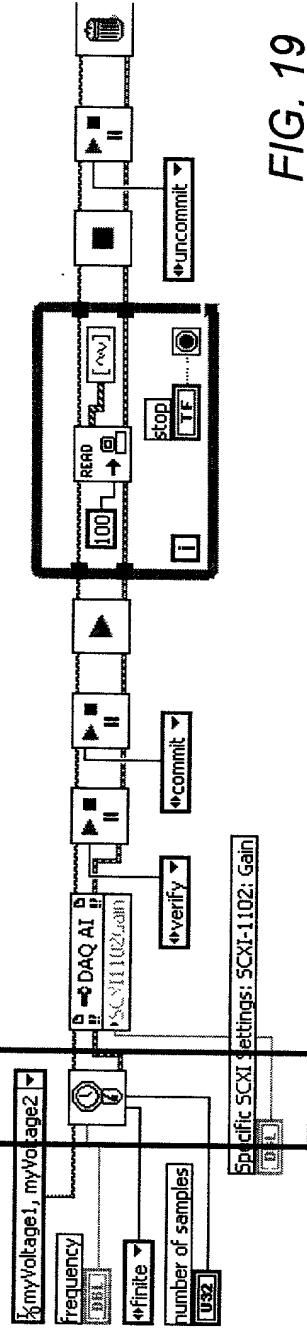


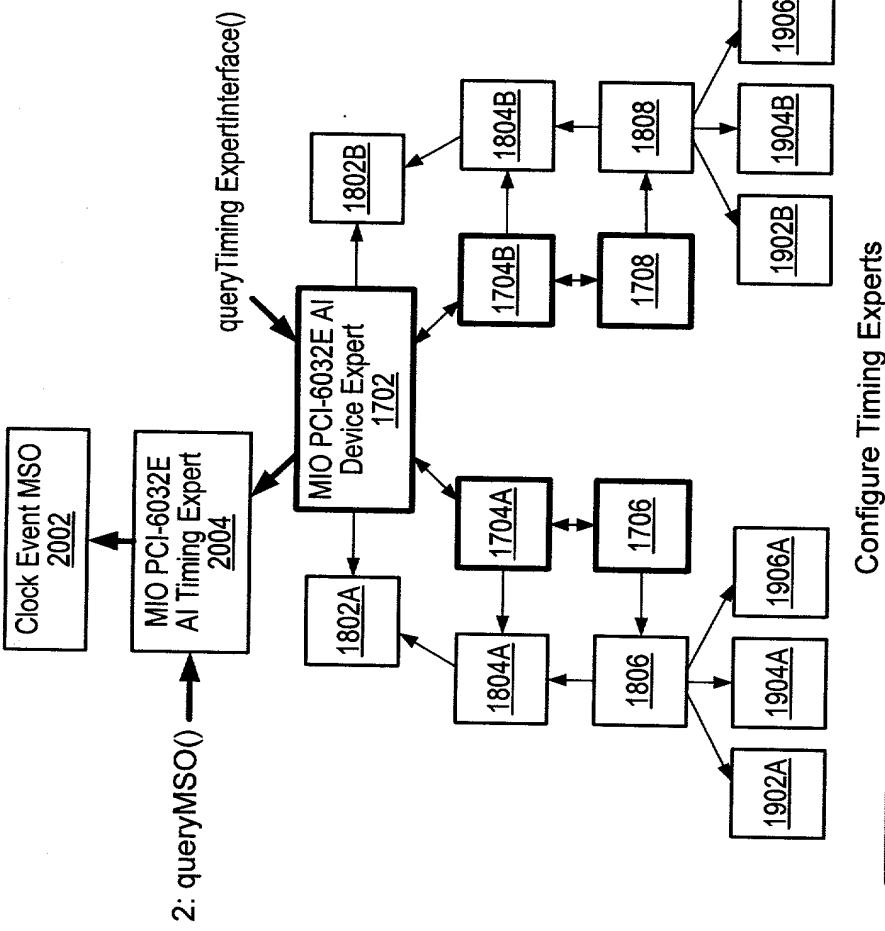
FIG. 18



Deserialize Named Channel MSOs



F/G. 19



Configure Timing Experts

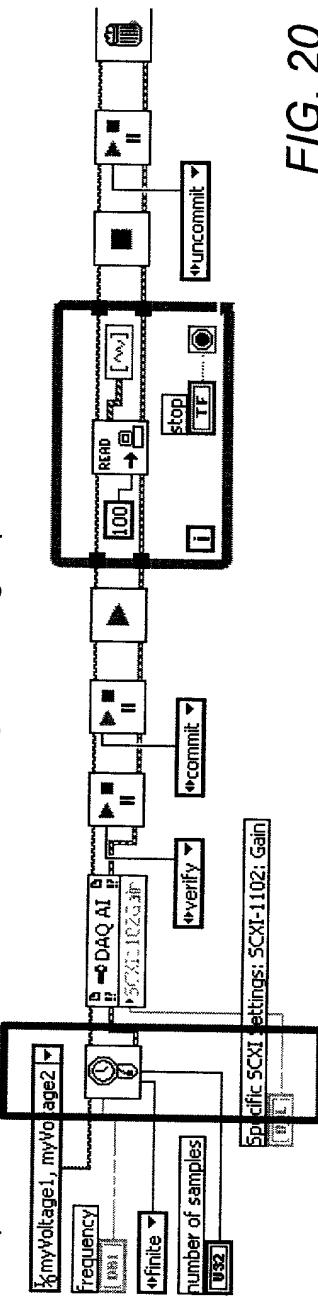


FIG. 20

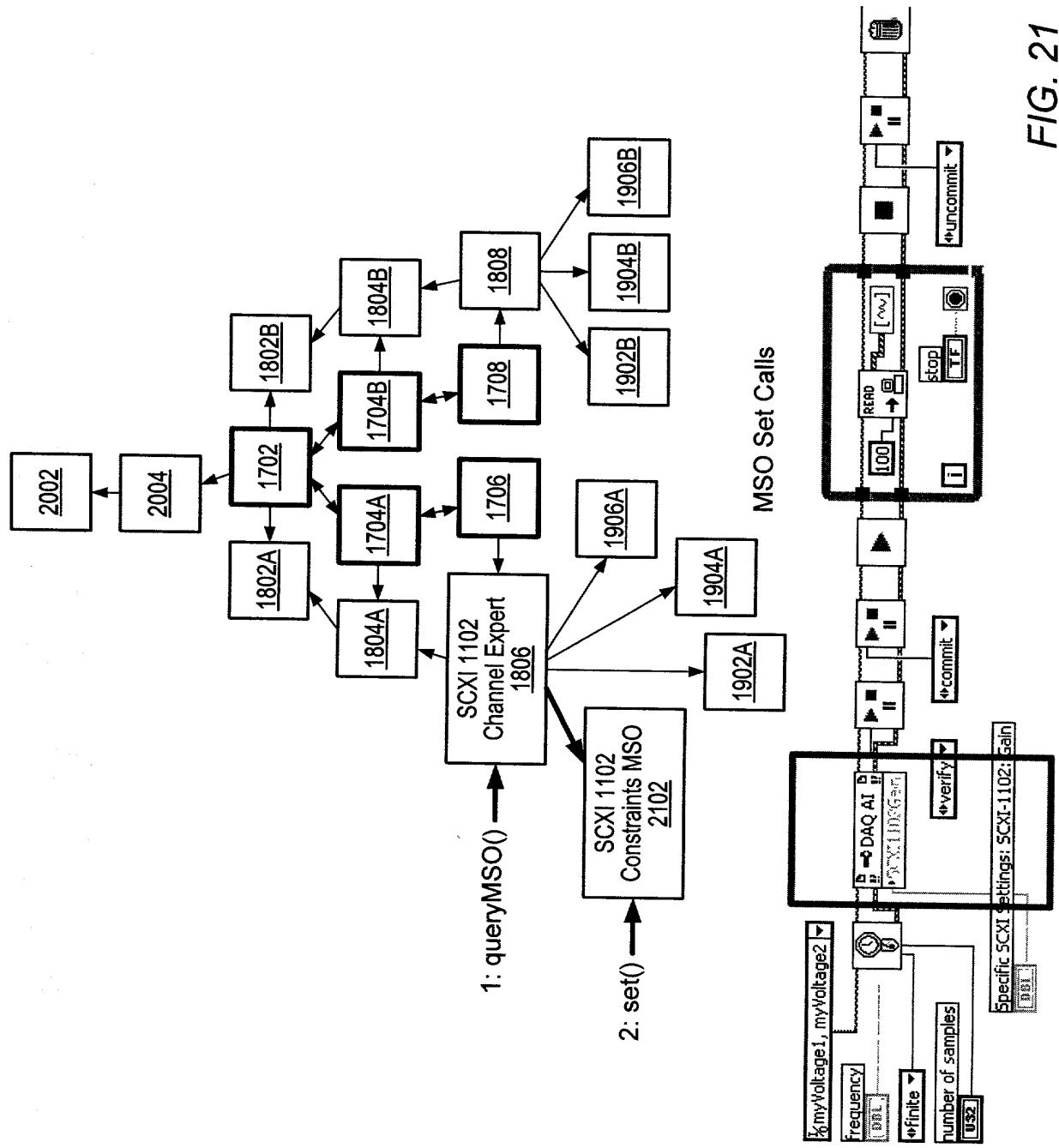


FIG. 21

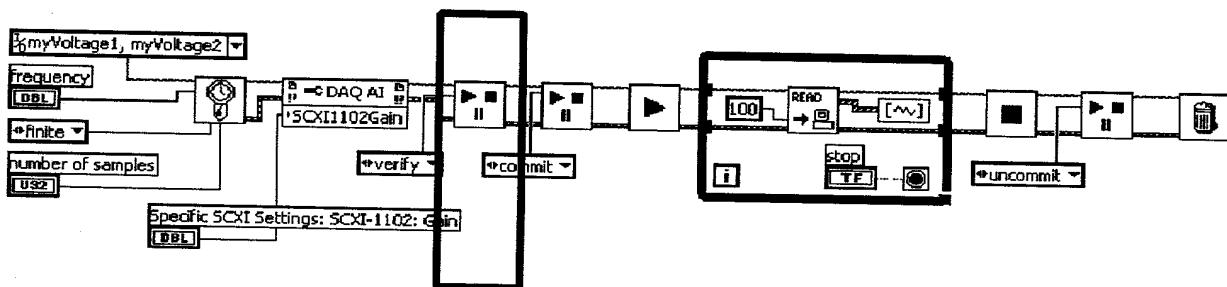
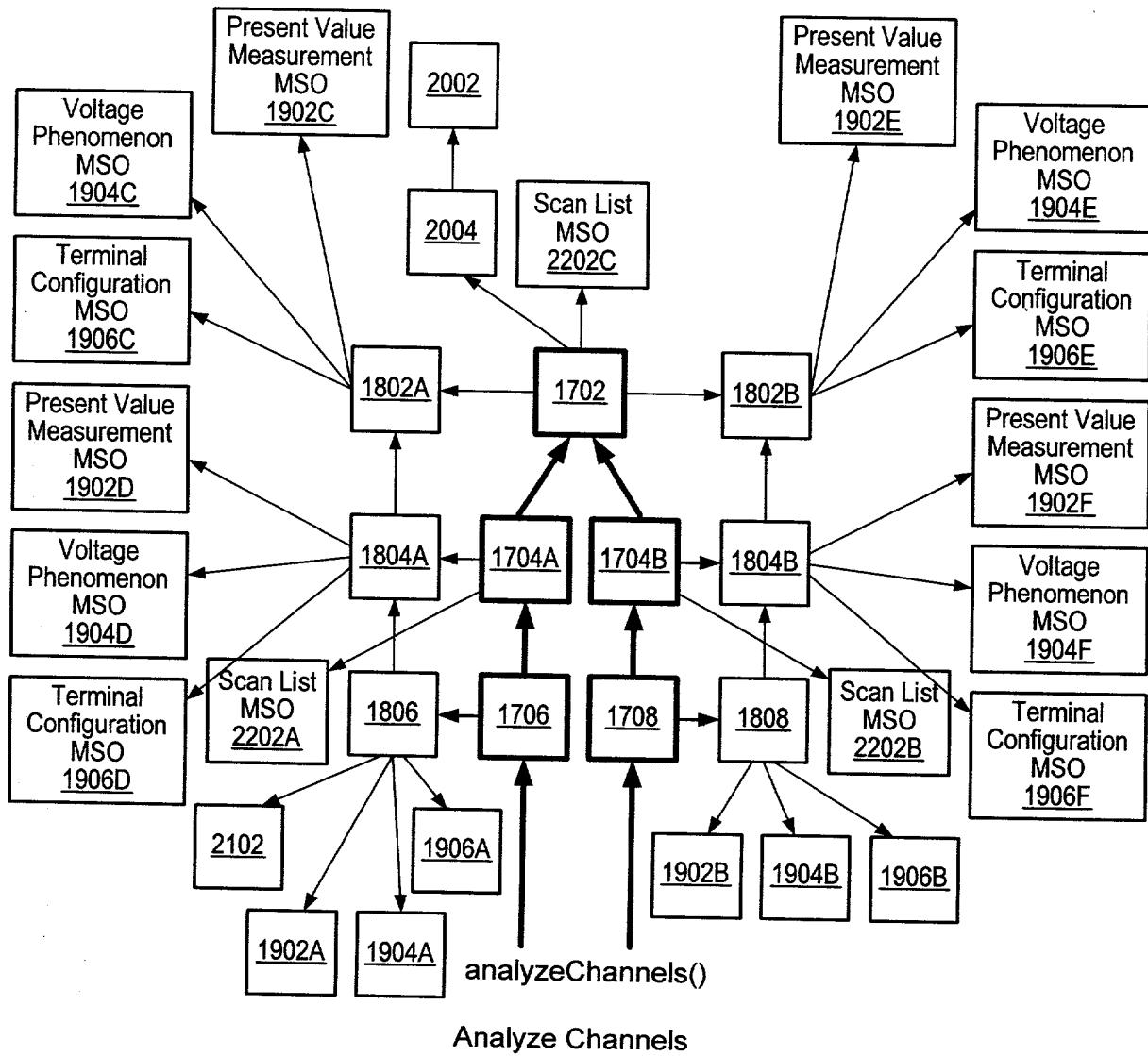


FIG. 22

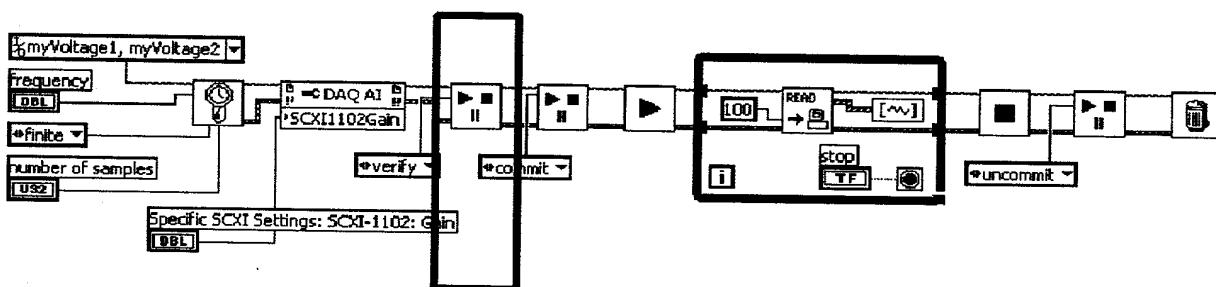
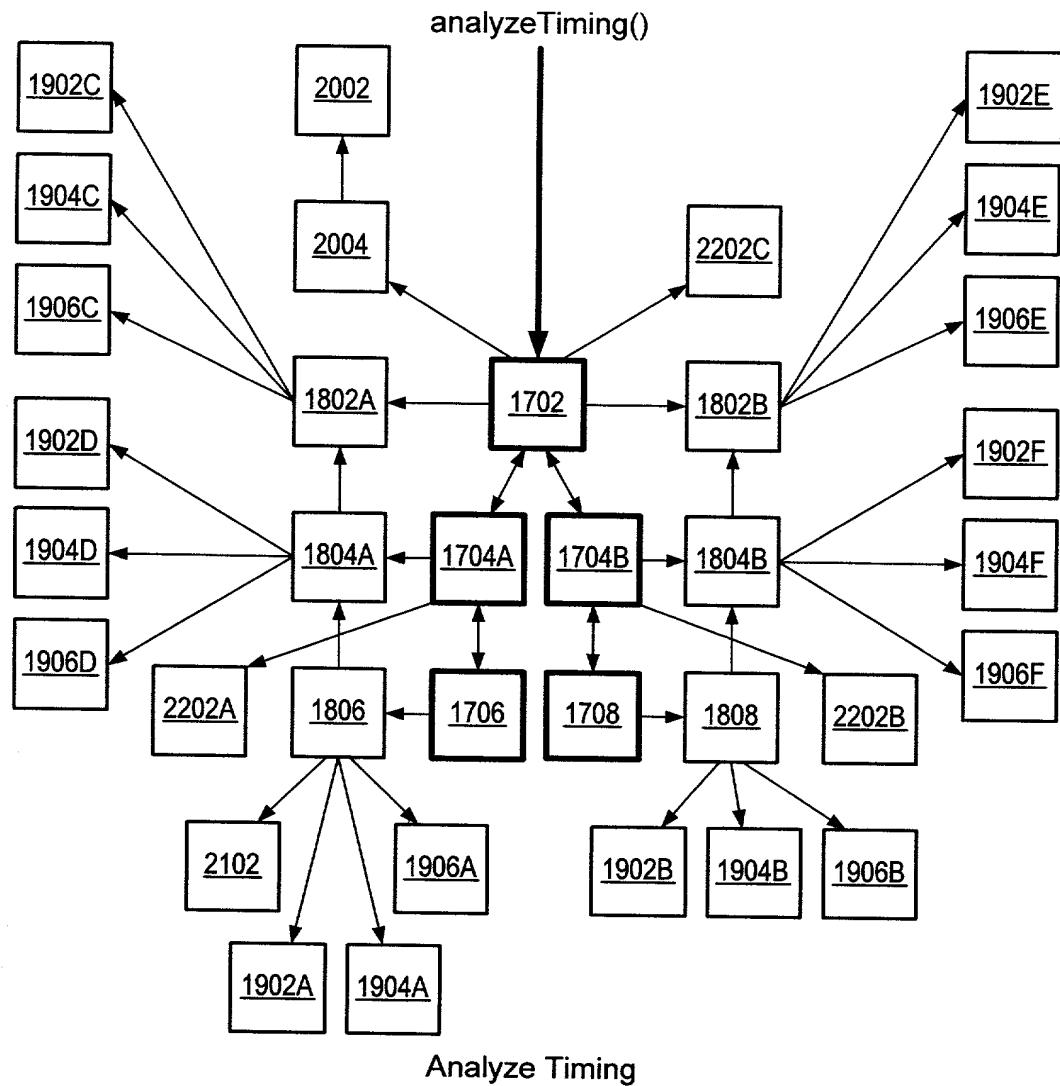


FIG. 23

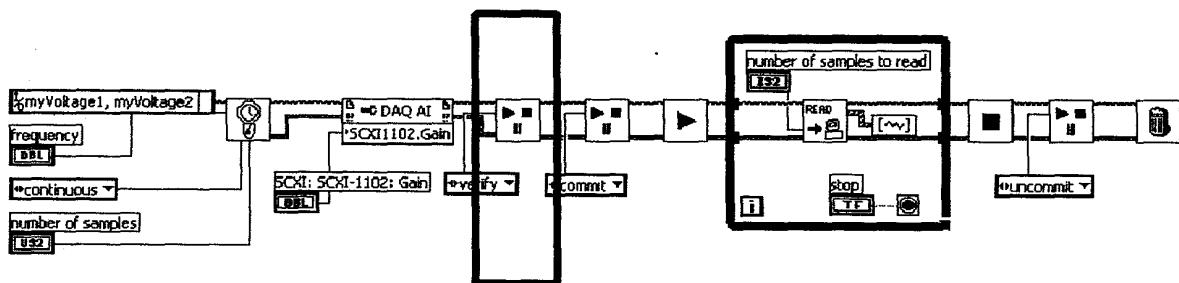
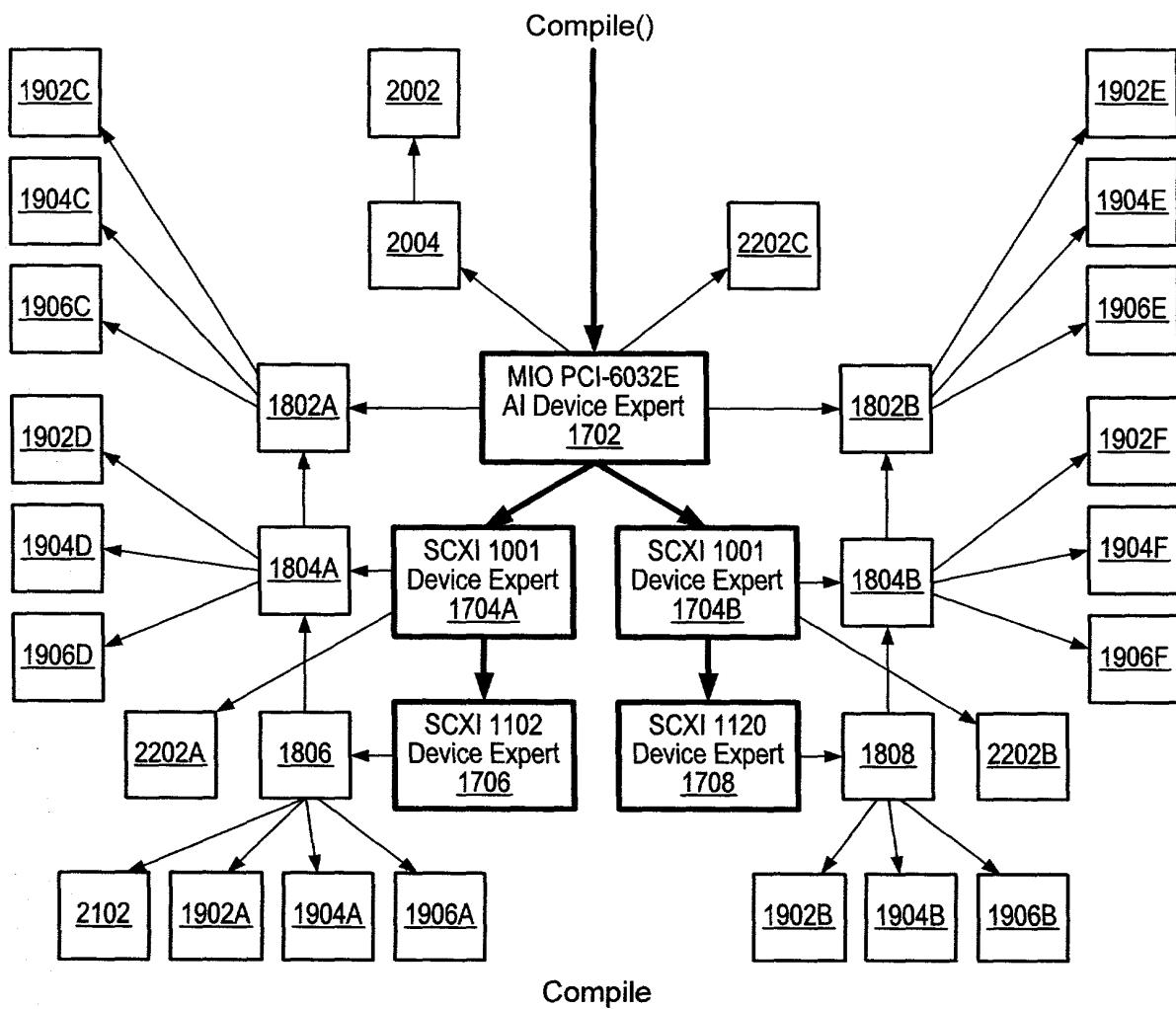


FIG. 24A

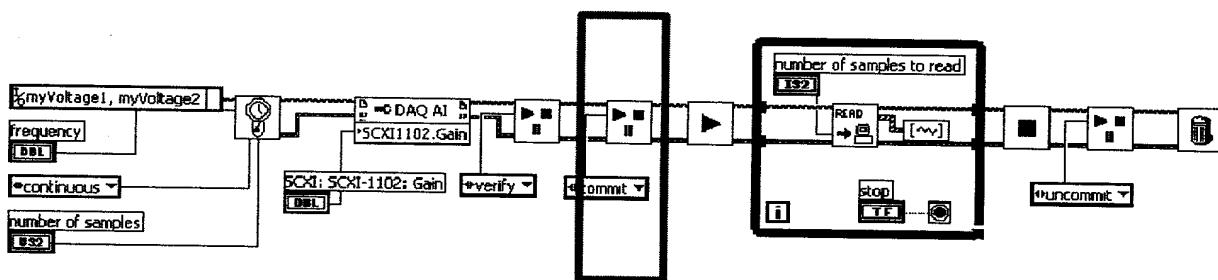
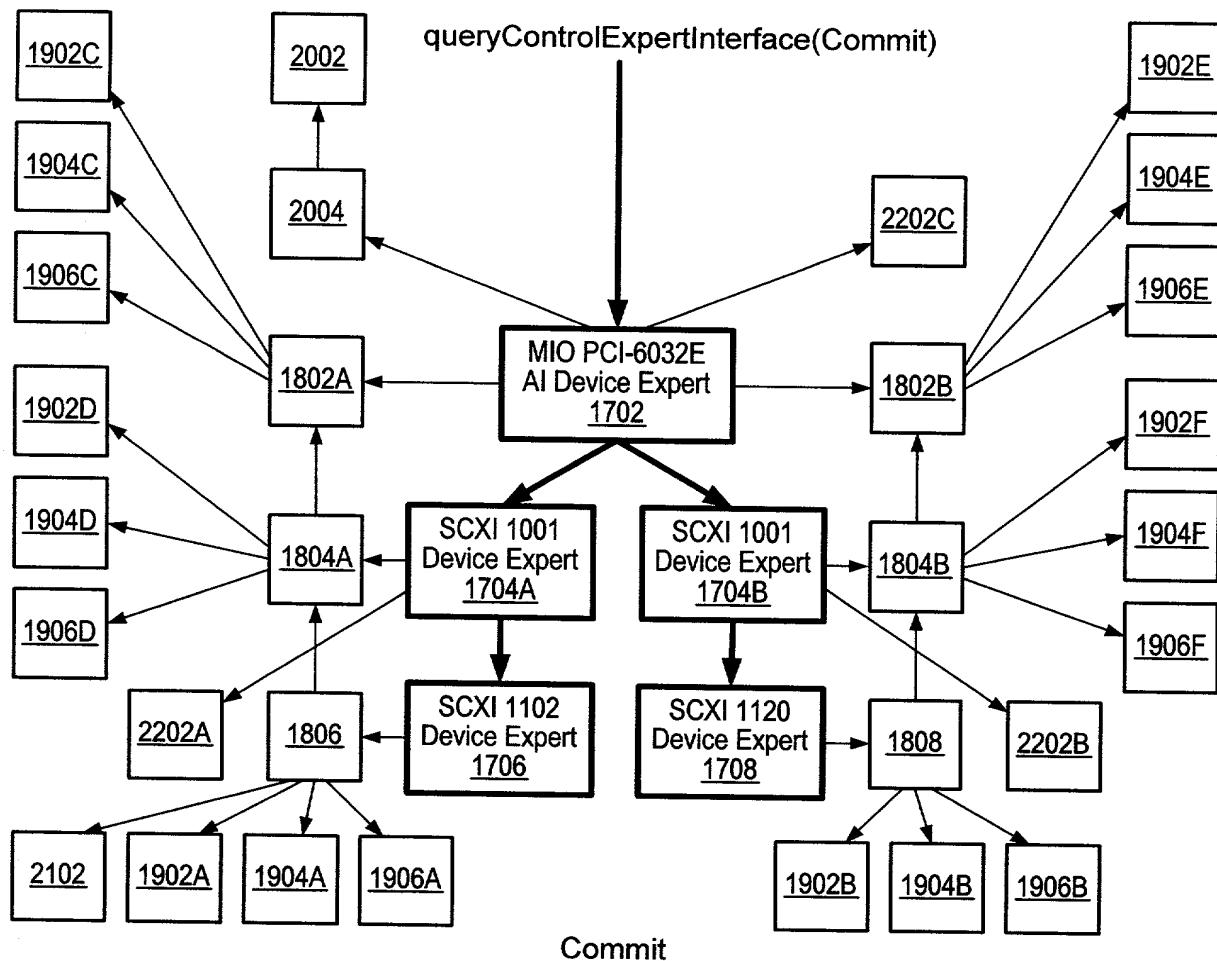


FIG. 24B

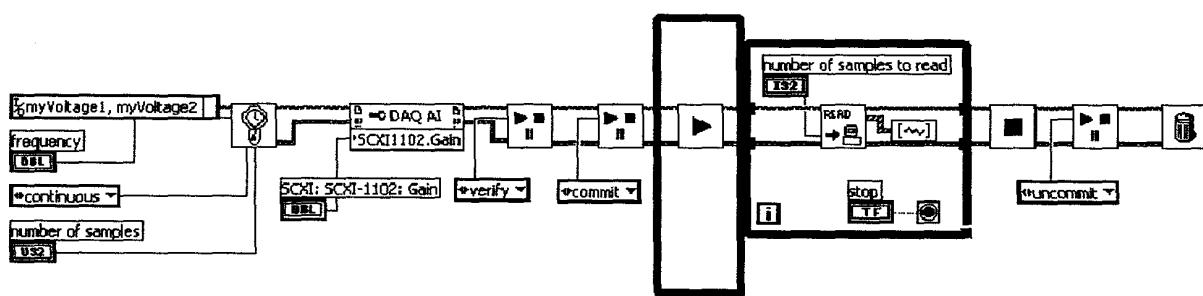
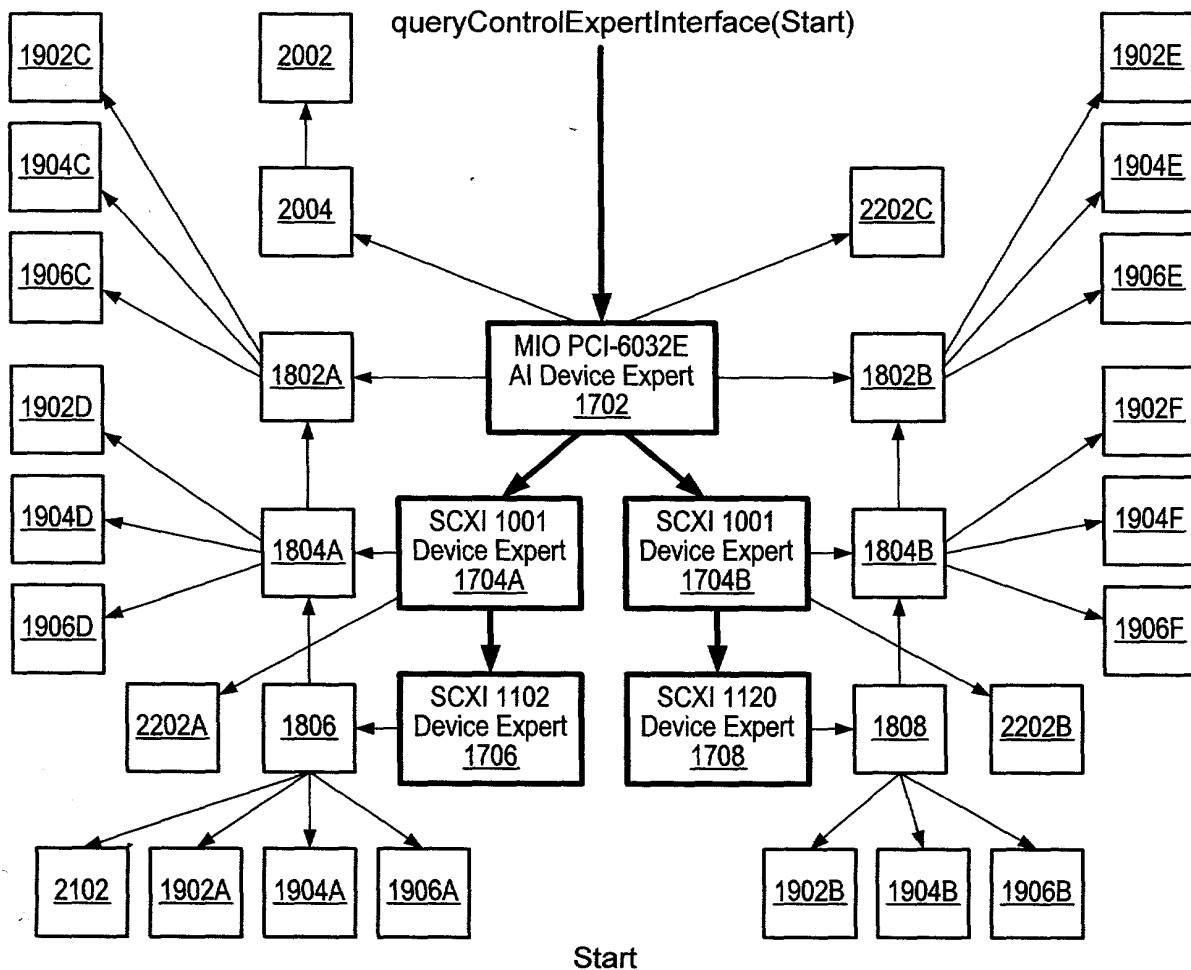
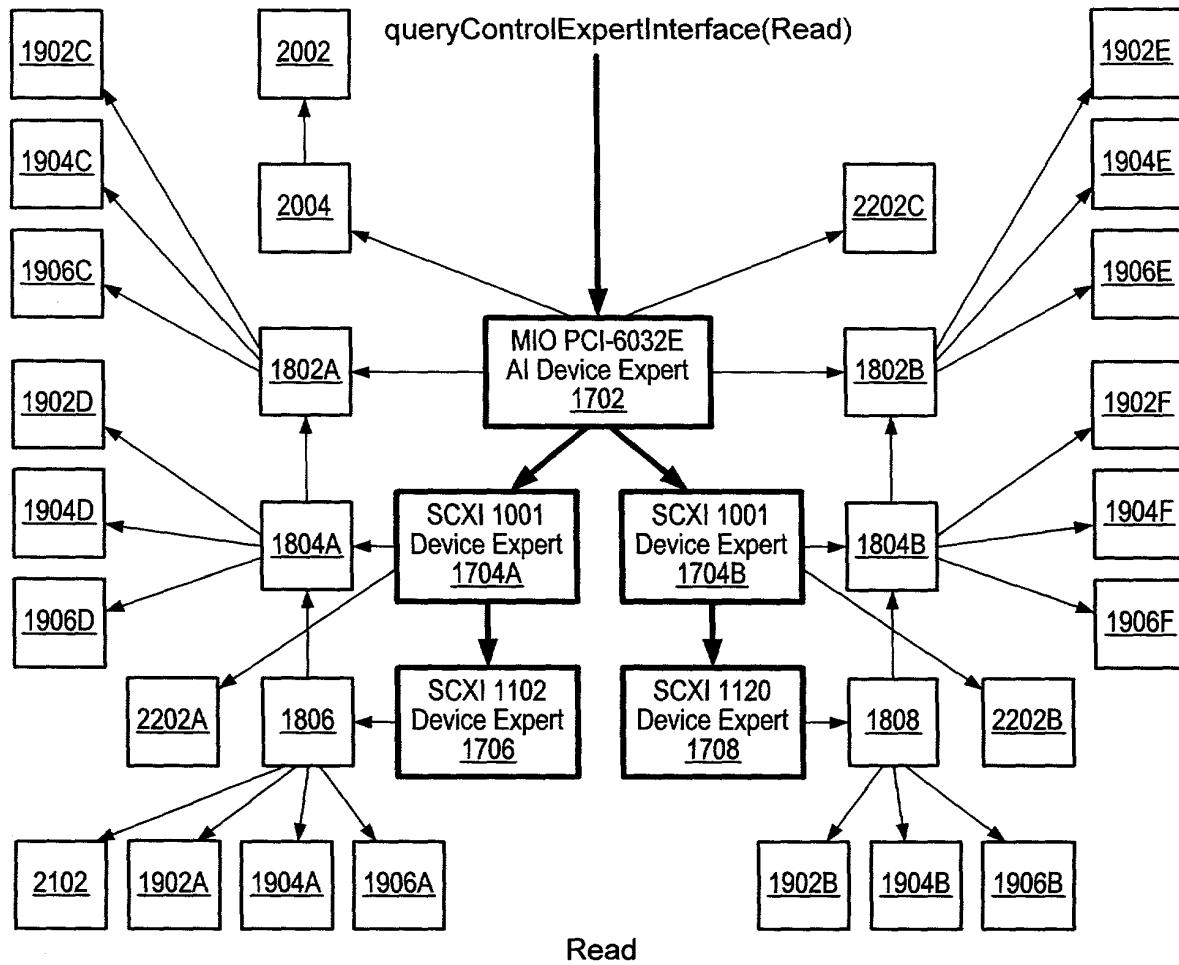


FIG. 24C

MIO PCI-6032E Configuration



Read

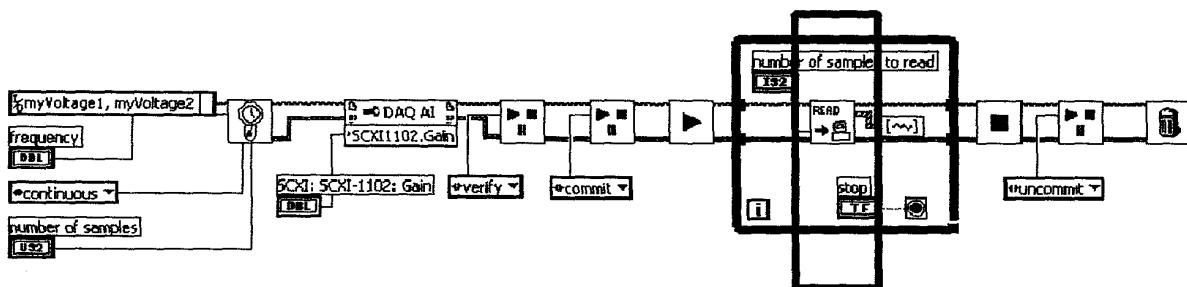


FIG. 24D

1...1000087932.m_CFE_18.CFG

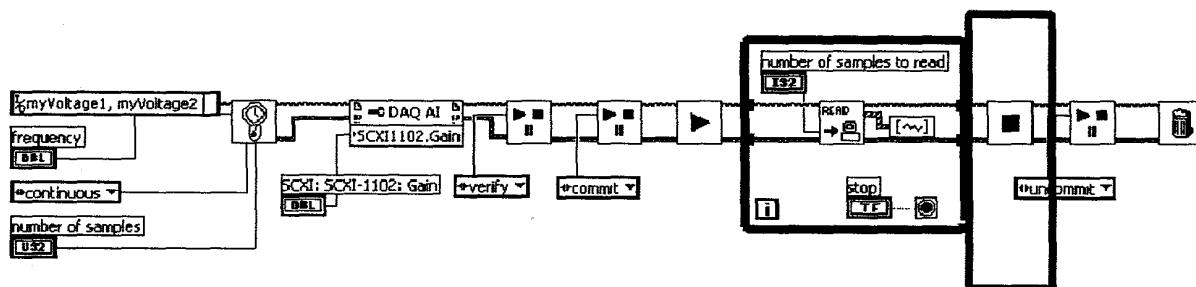
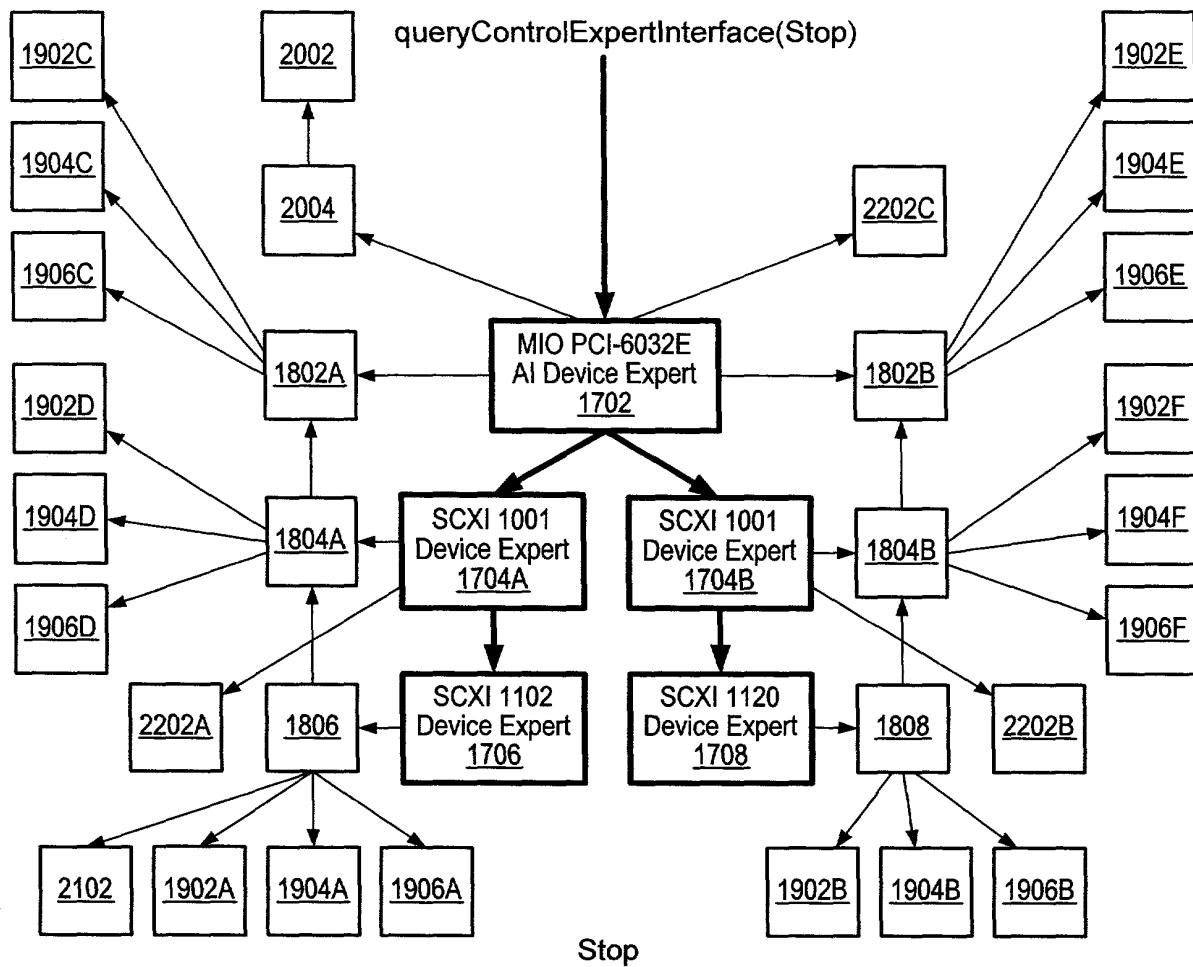


FIG. 24E

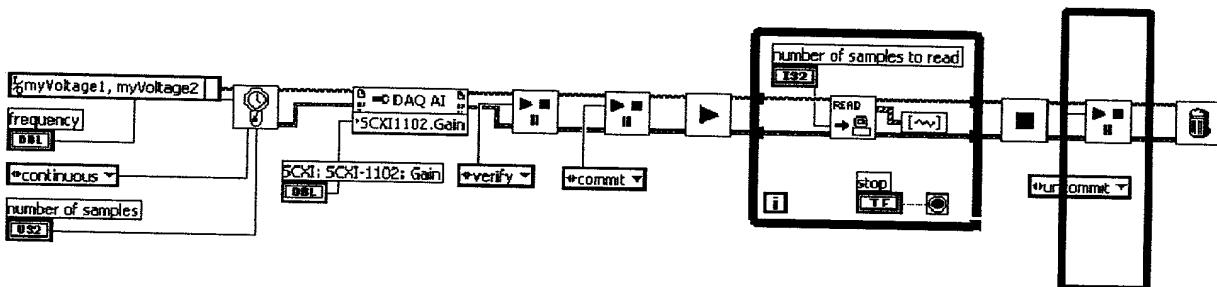
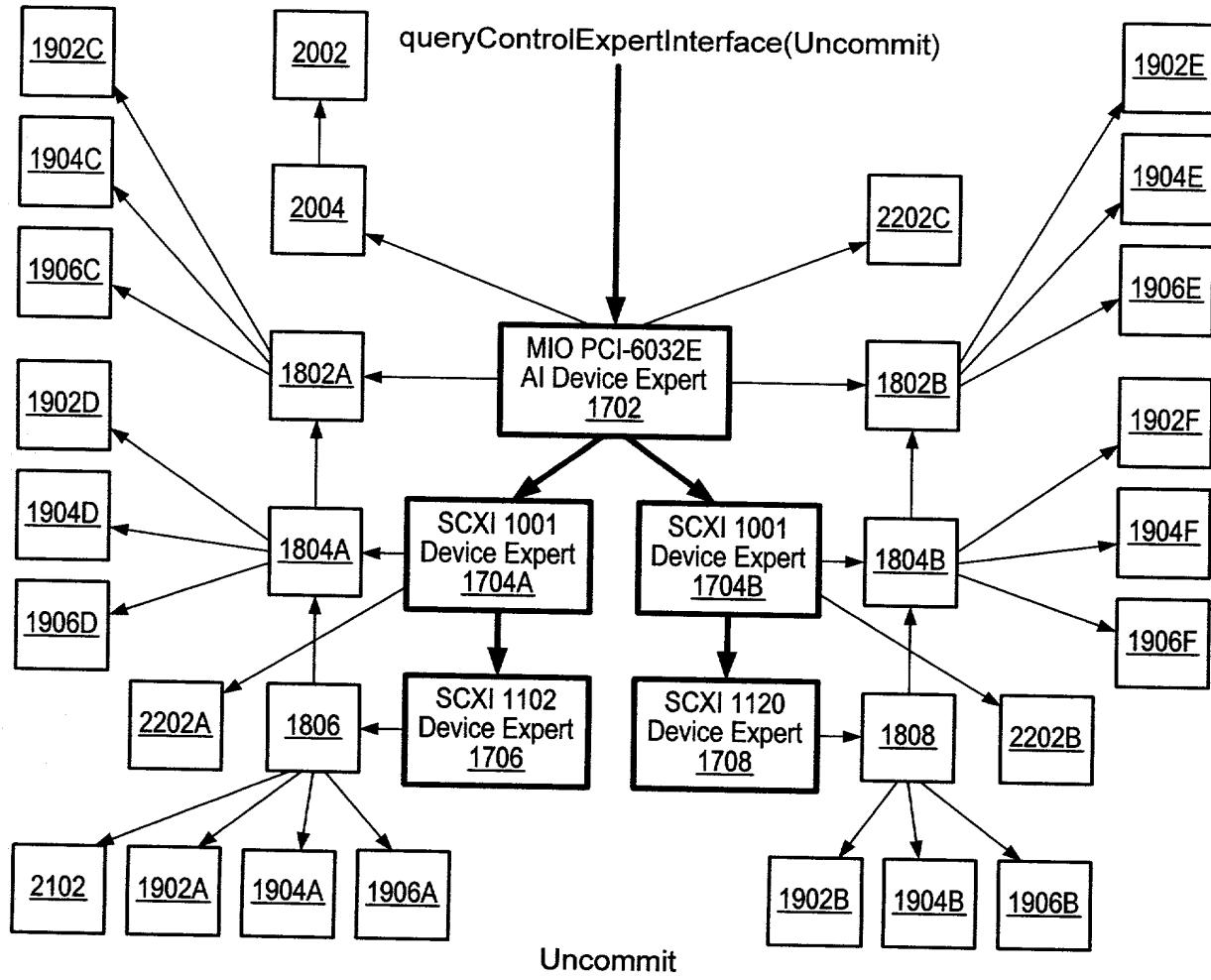


FIG. 24F

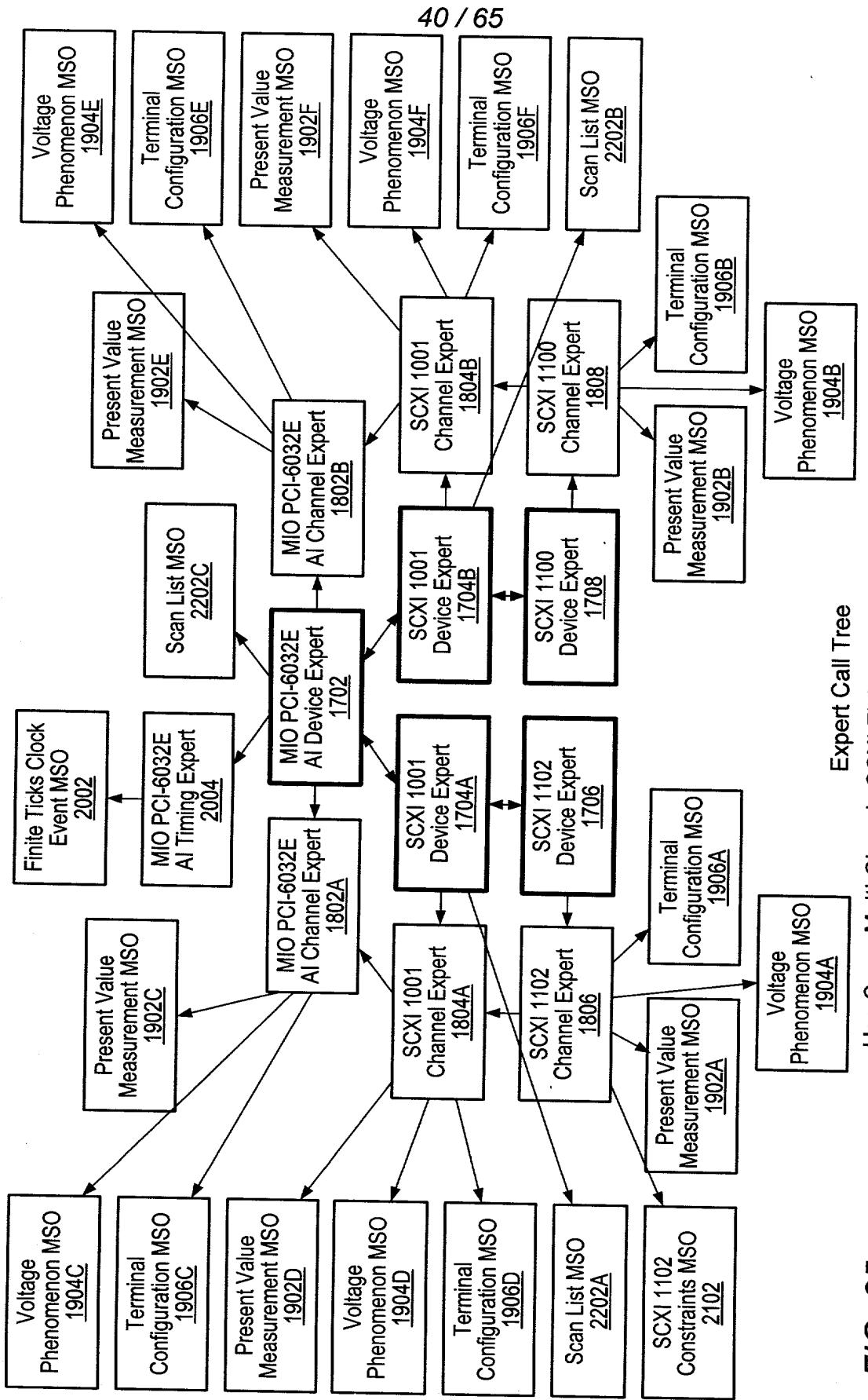


FIG. 25

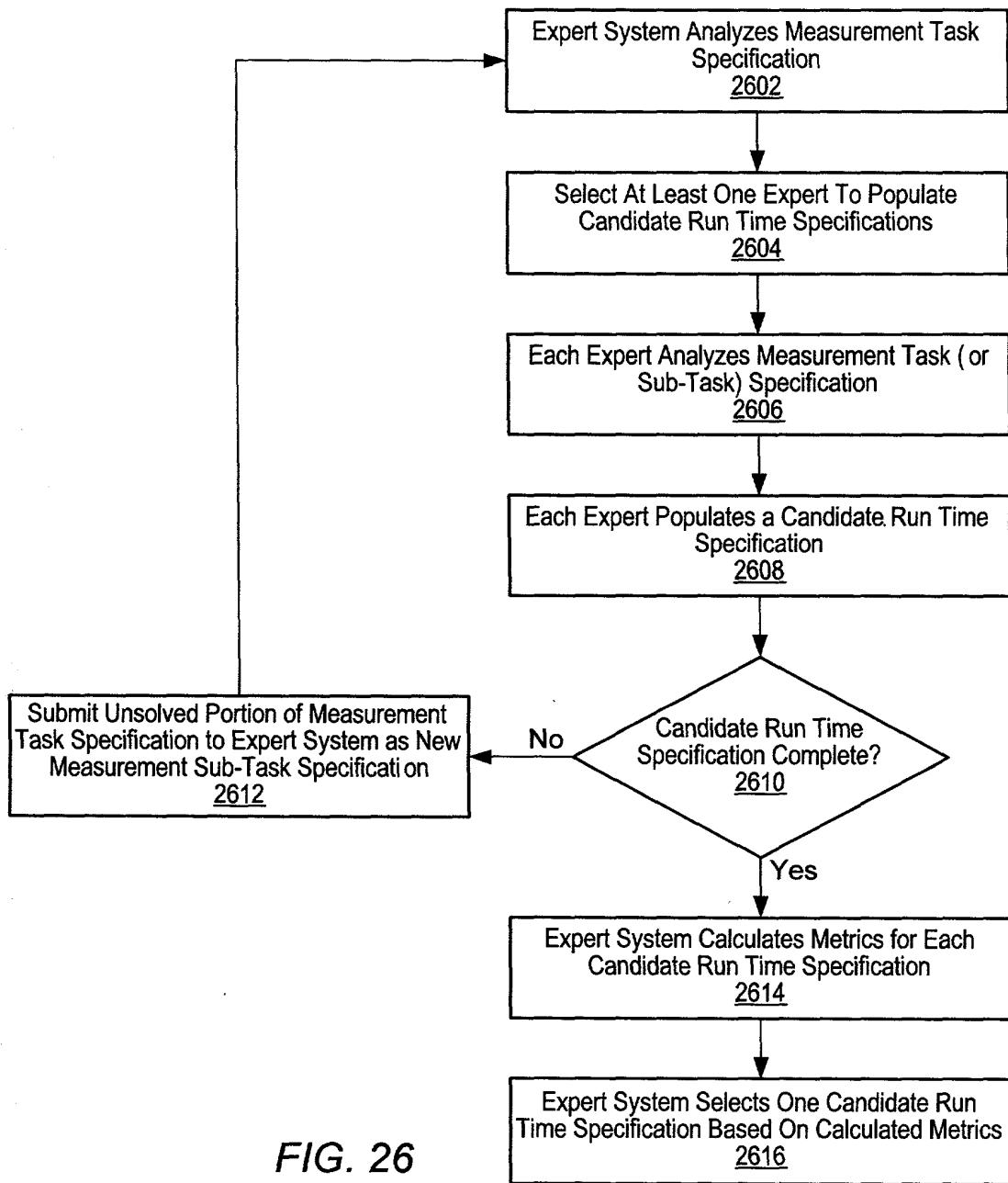


FIG. 26

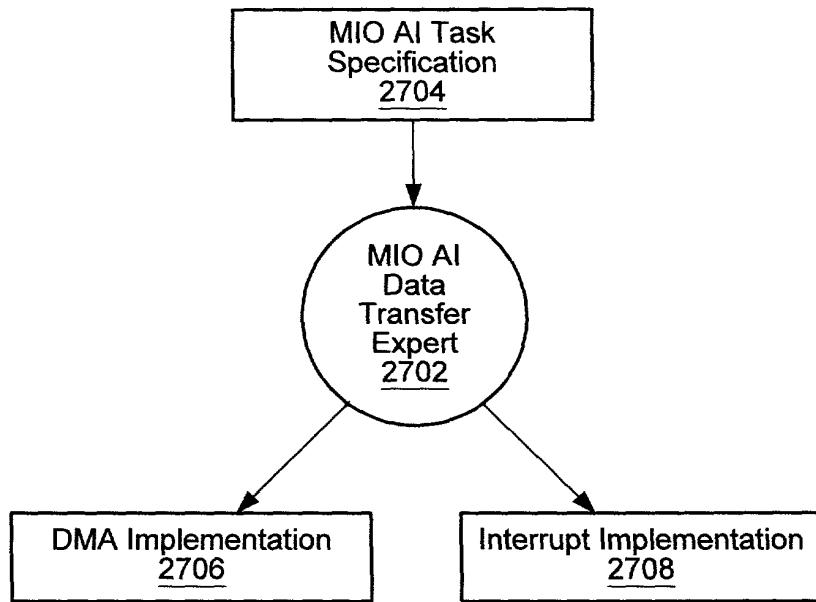


FIG. 27

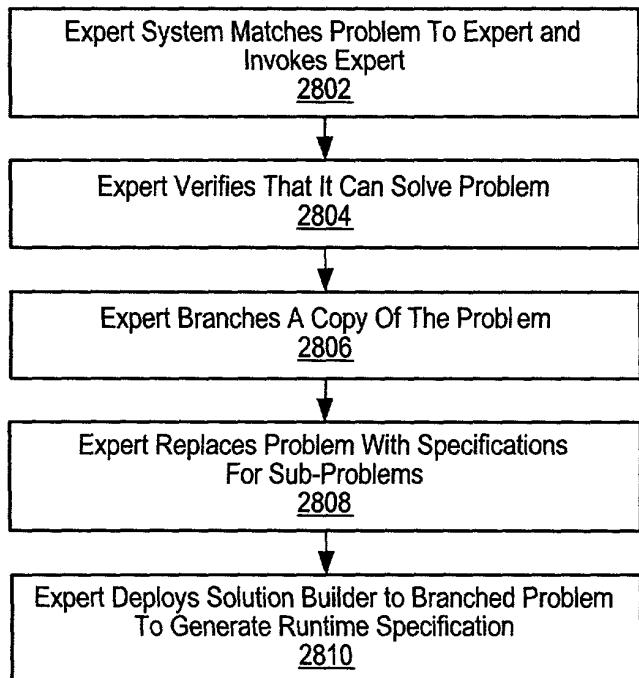


FIG. 28

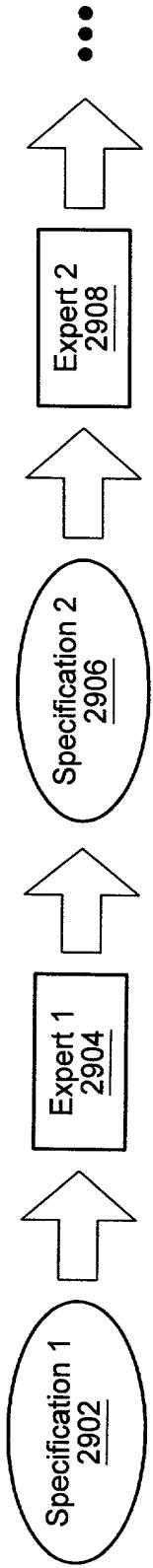


FIG. 29

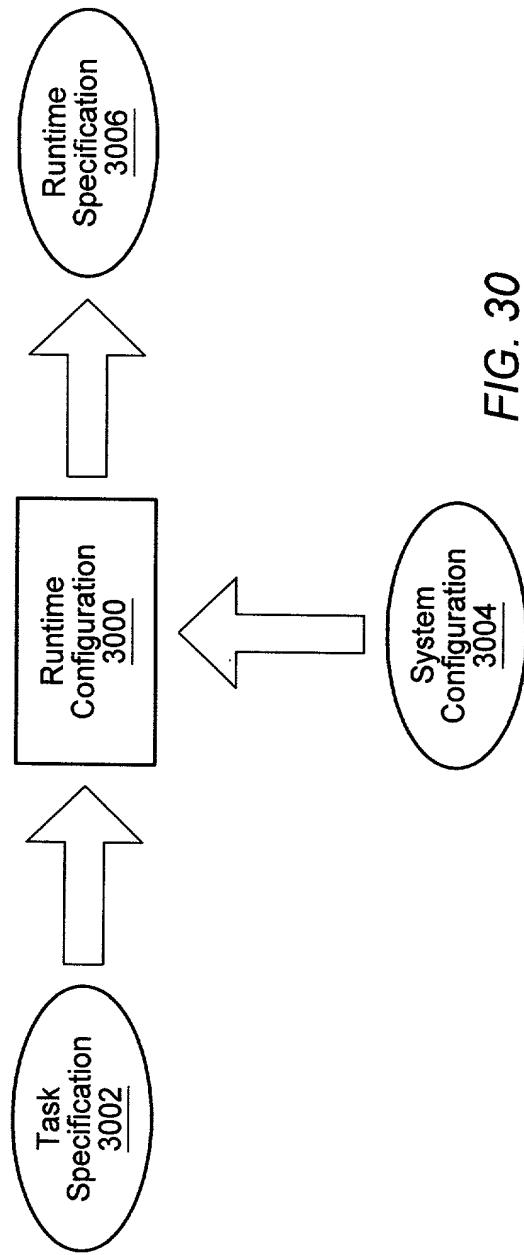


FIG. 30

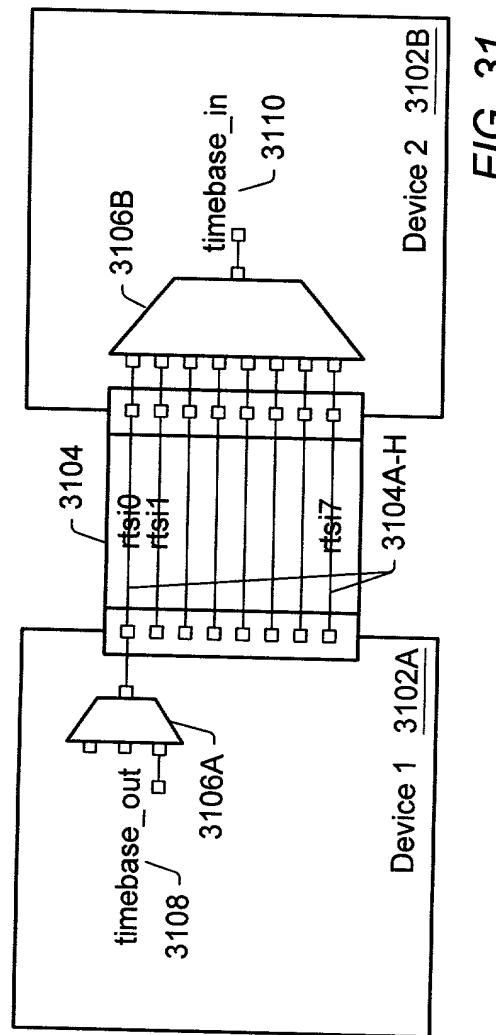


FIG. 31

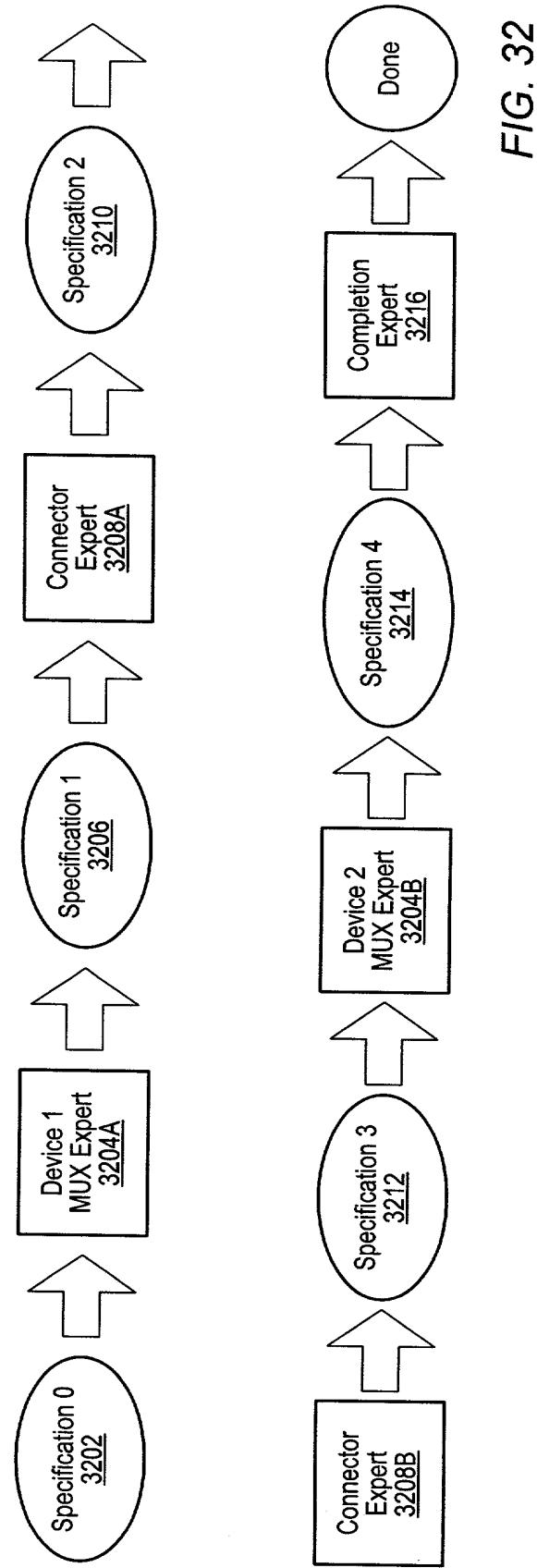


FIG. 32

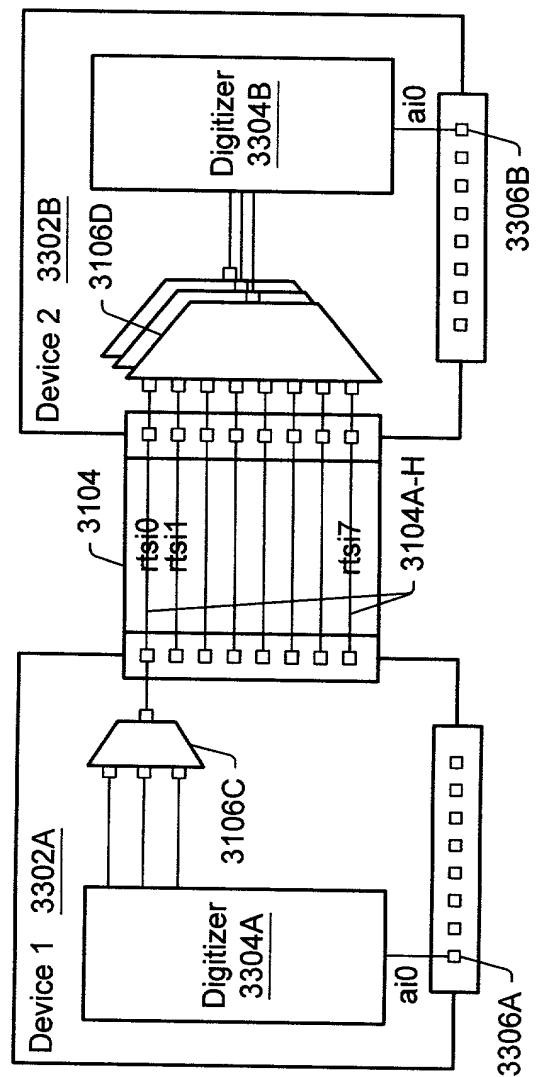


FIG. 33

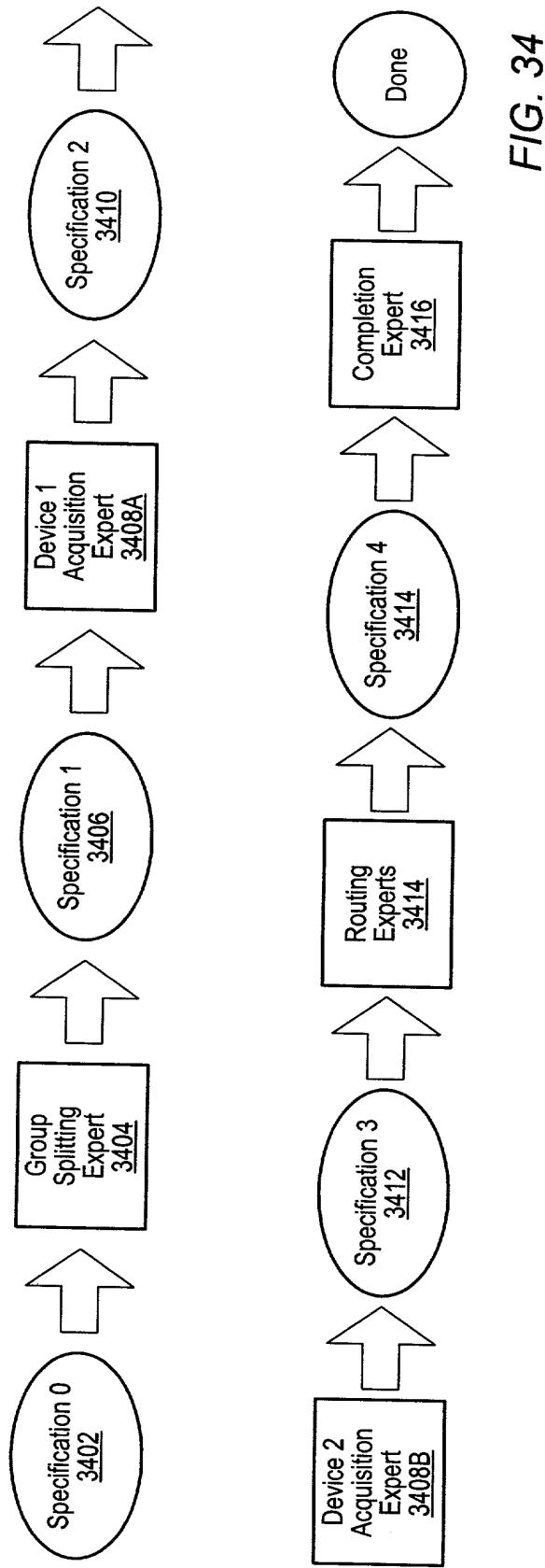


FIG. 34

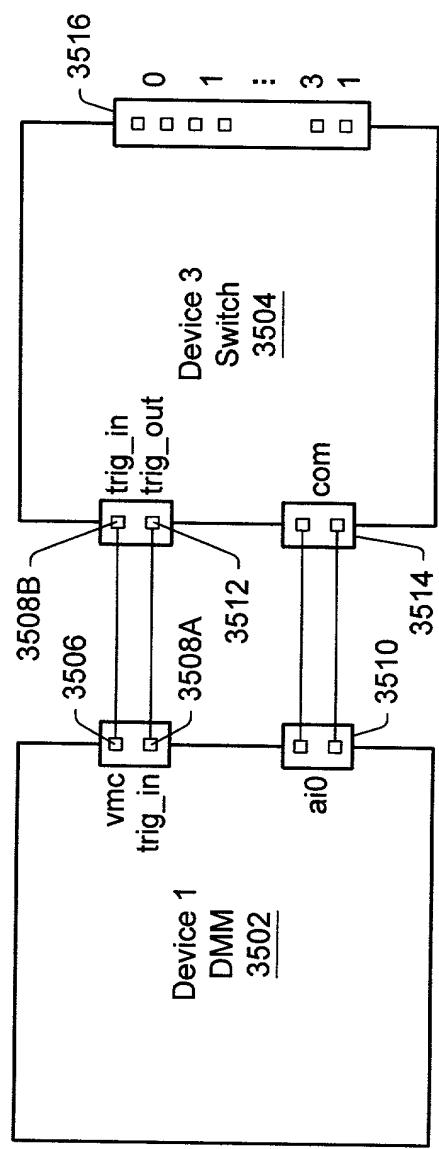


FIG. 35

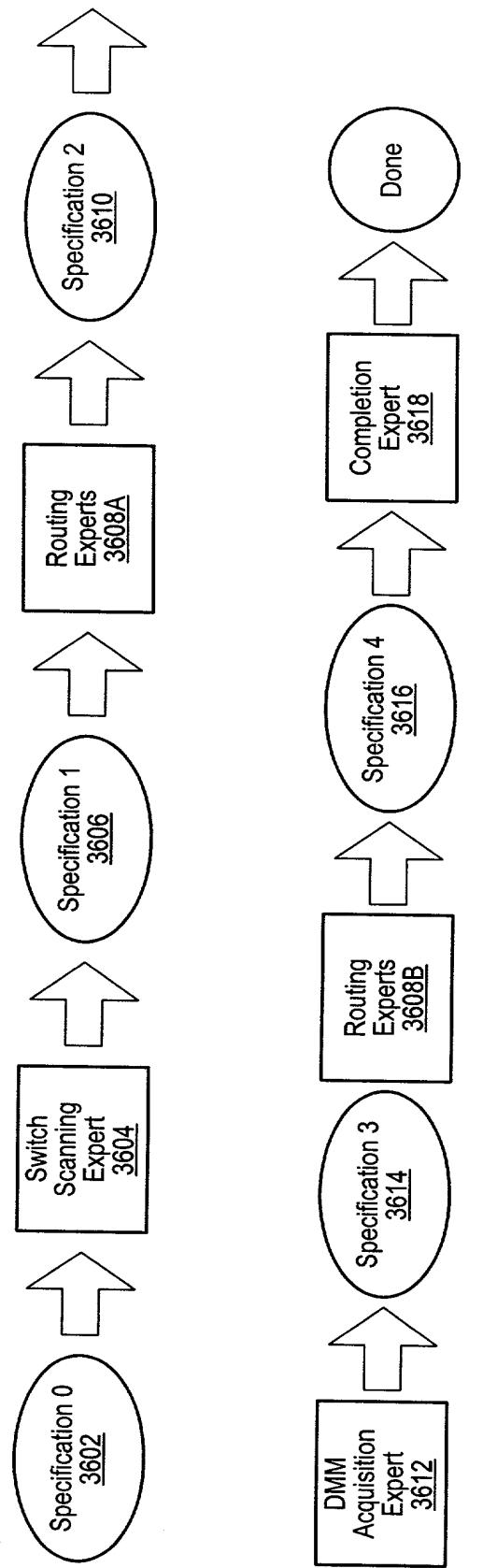
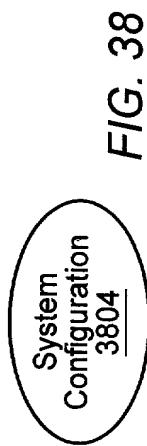
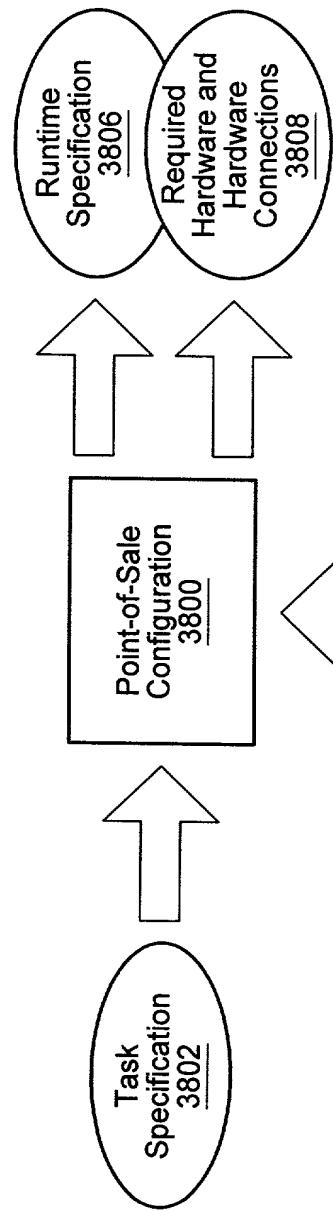
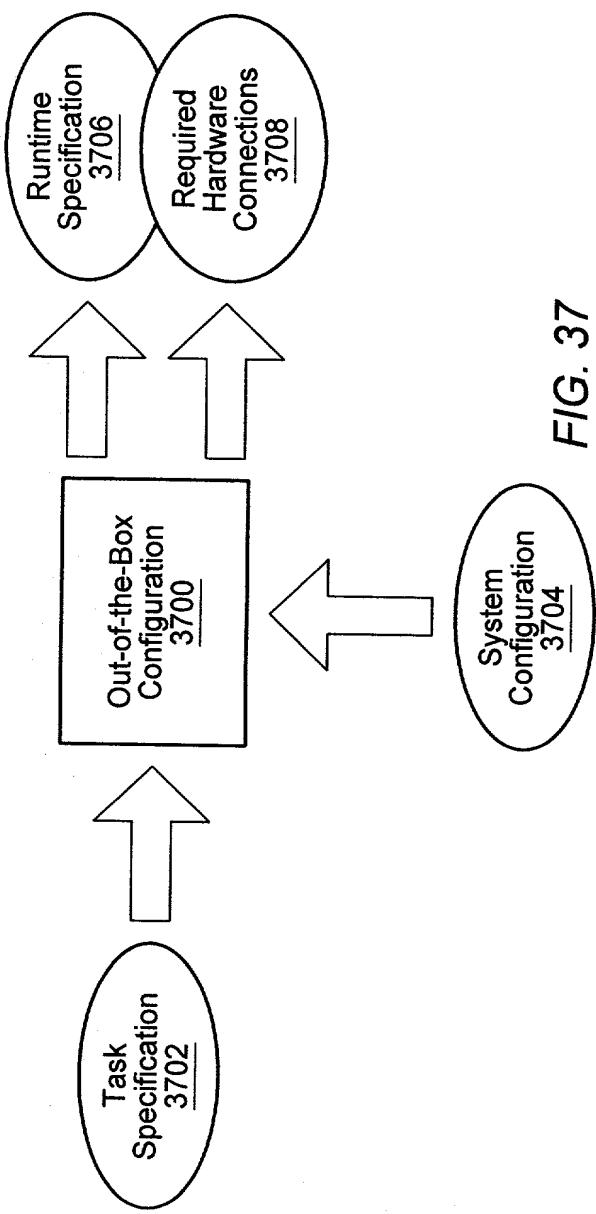


FIG. 36



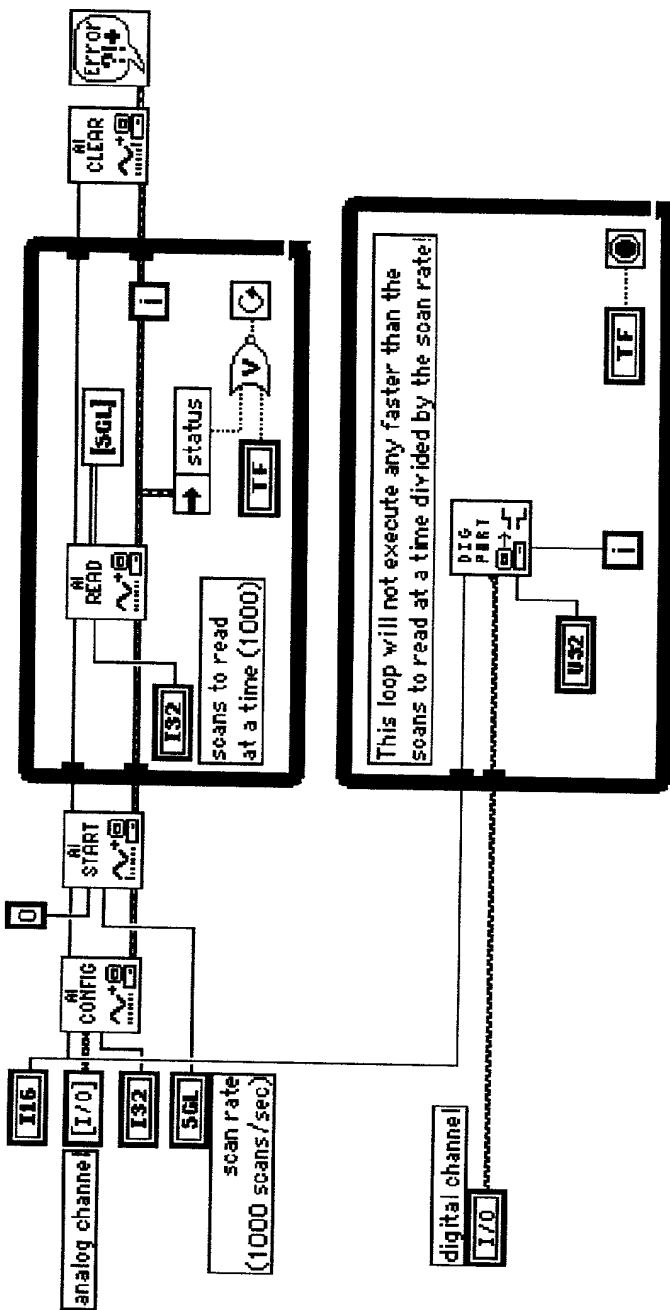


FIG. 39A
(Prior Art)

Simultaneous Buffered Analog Input And Single Point Digital Output With Single-Threaded Driver (Prior Art)

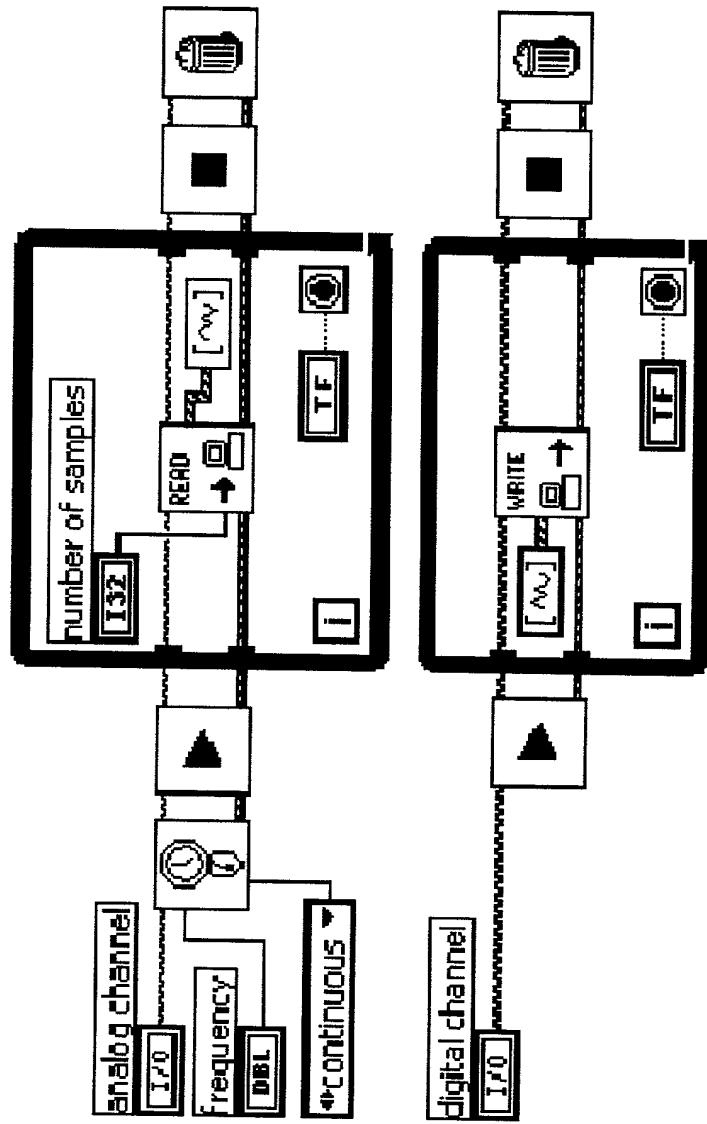


FIG. 39B
Simultaneous Buffered Analog Input And Single Point
Digital Output With Multi-Threaded Driver

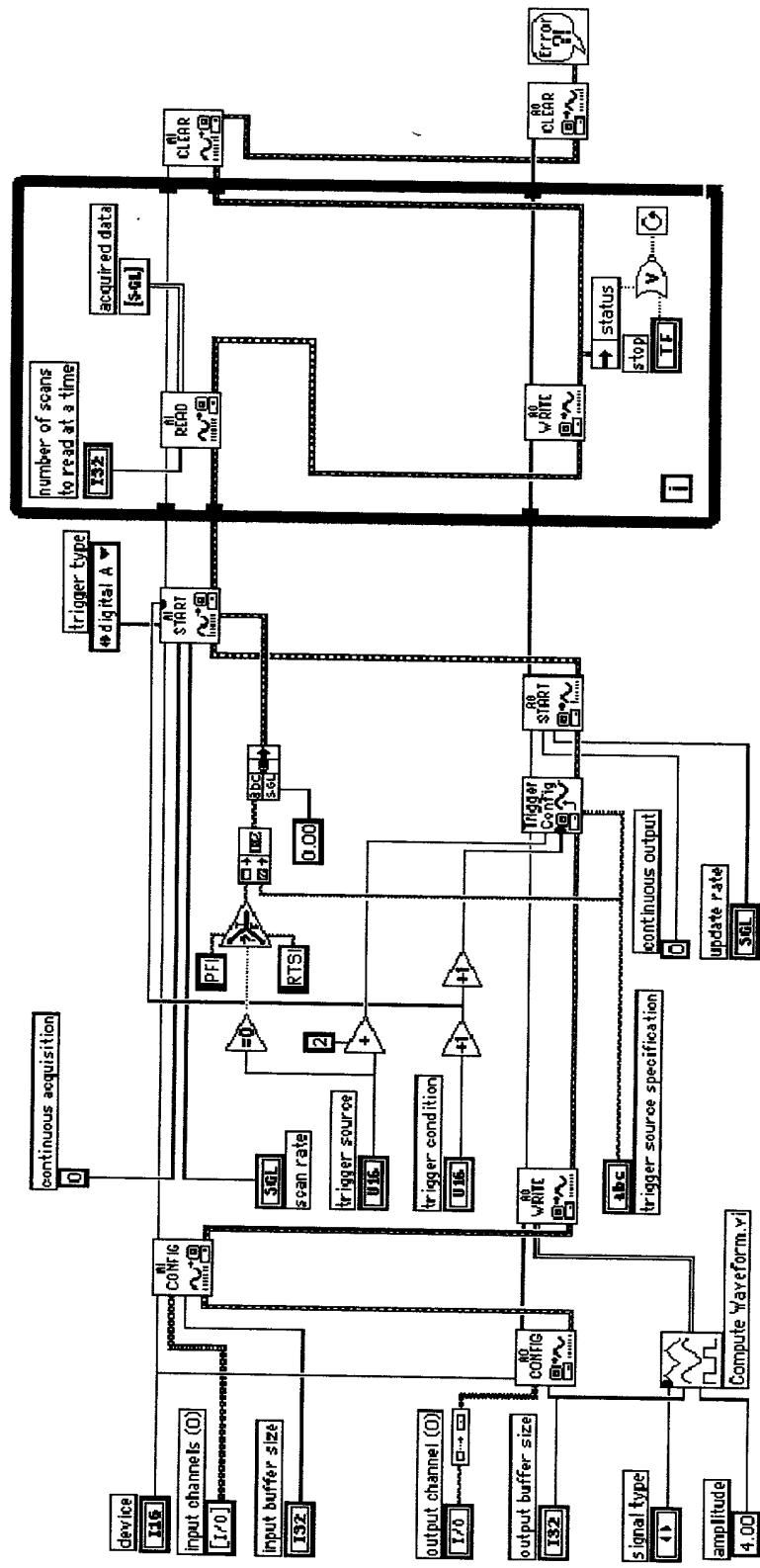


FIG. 40A

Simultaneous Triggered Buffered AI/AO (Prior Art)

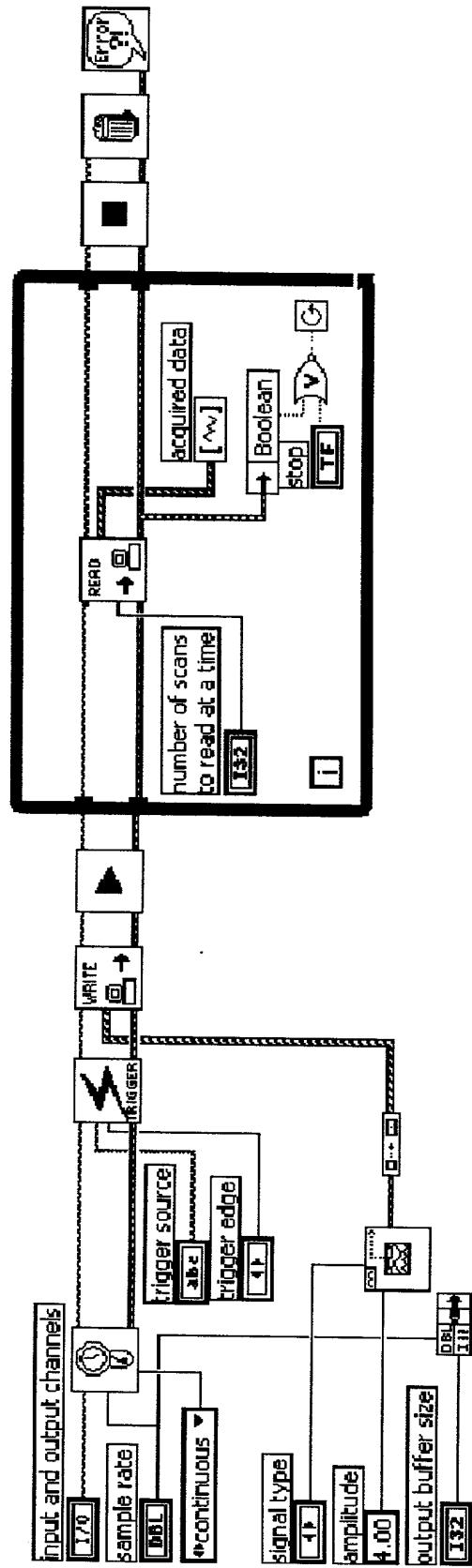


FIG. 40B

Simultaneous Triggered Buffered AI/AO

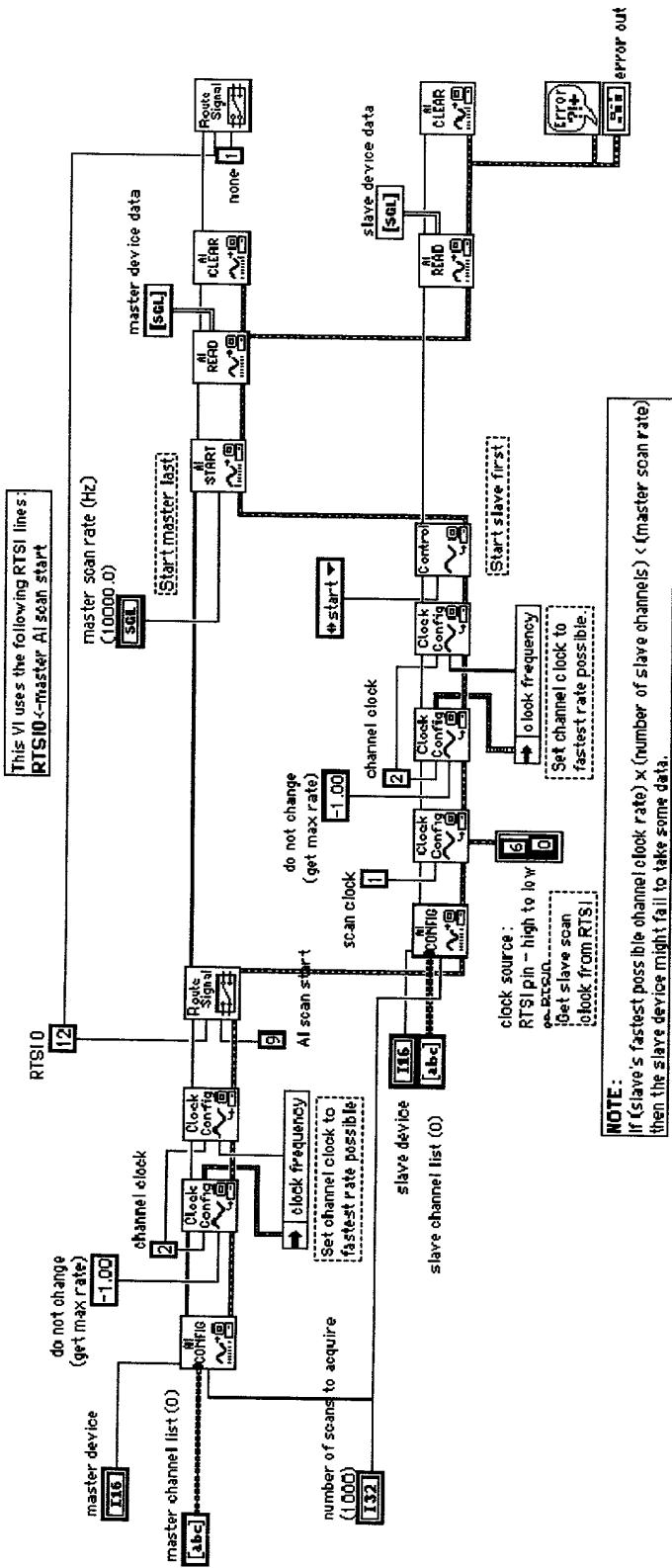
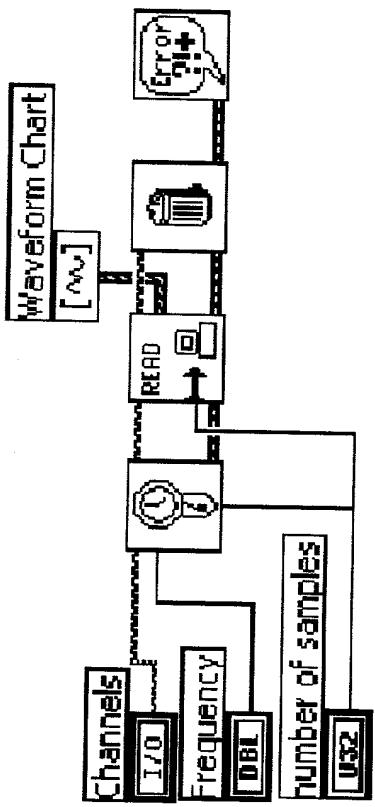


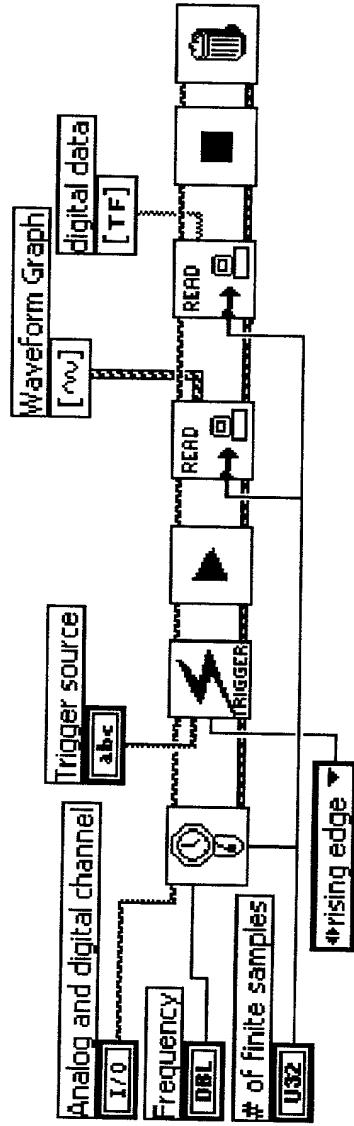
FIG. 41A

Sharing Scan Clock Across Two E-Series Devices (Prior Art)



Sharing Scan Clock Across Two E-Series Devices

FIG. 41B



Sharing Clock And Trigger, Buffered AI & DI

FIG. 42

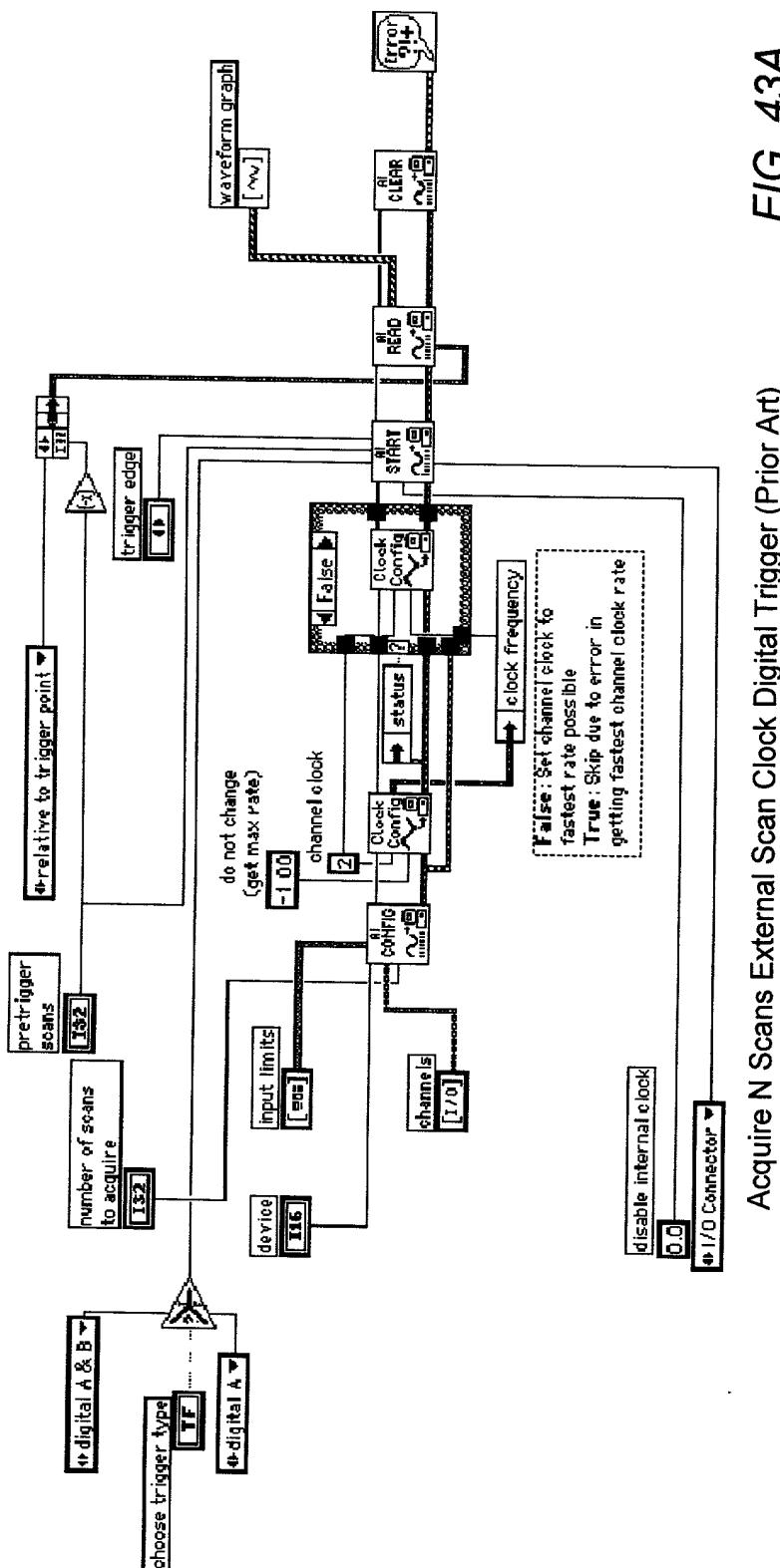


FIG. 43A
(Prior Art)

Acquire N Scans External Scan Clock Digital Trigger (Prior Art)

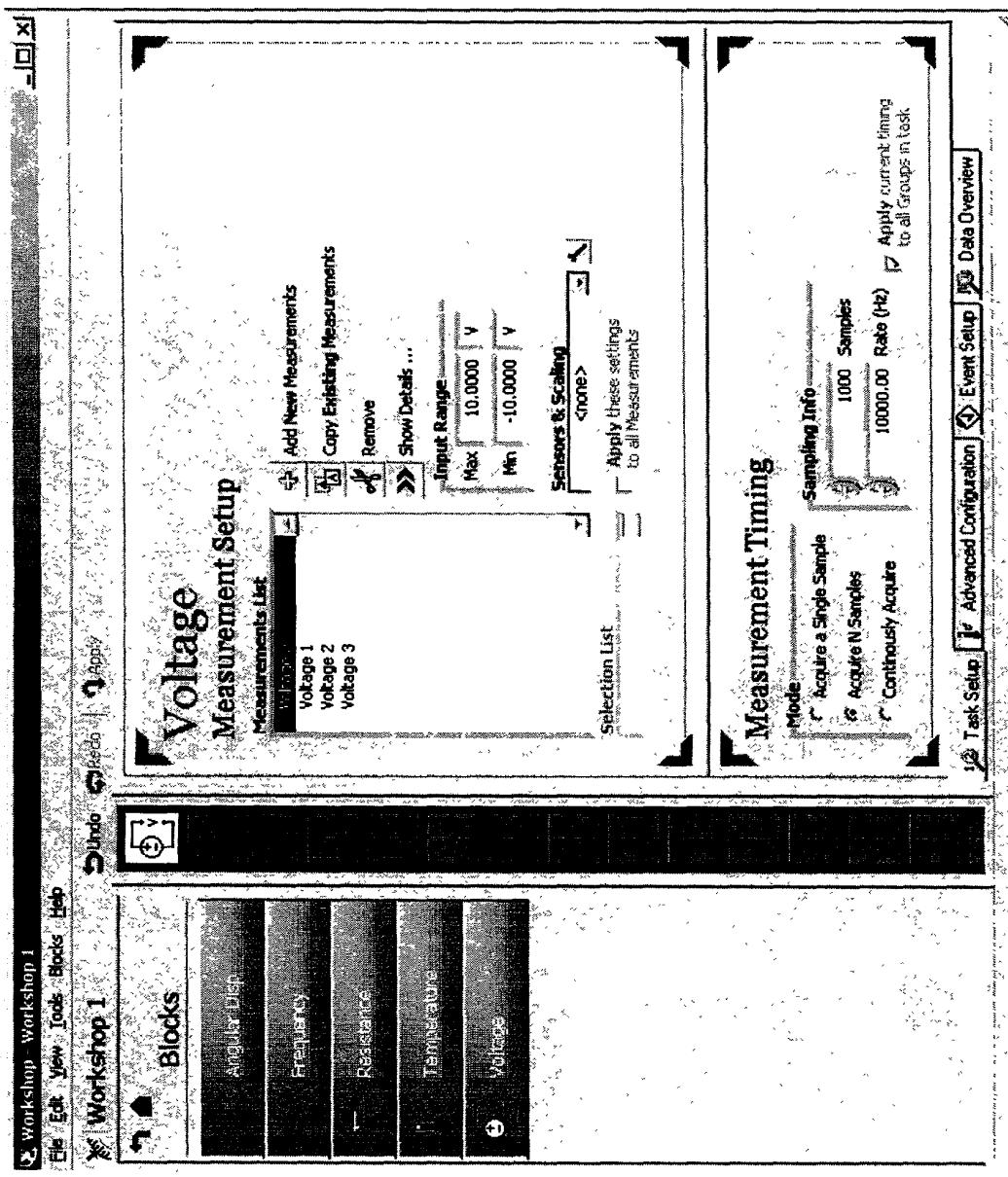


FIG. 43B

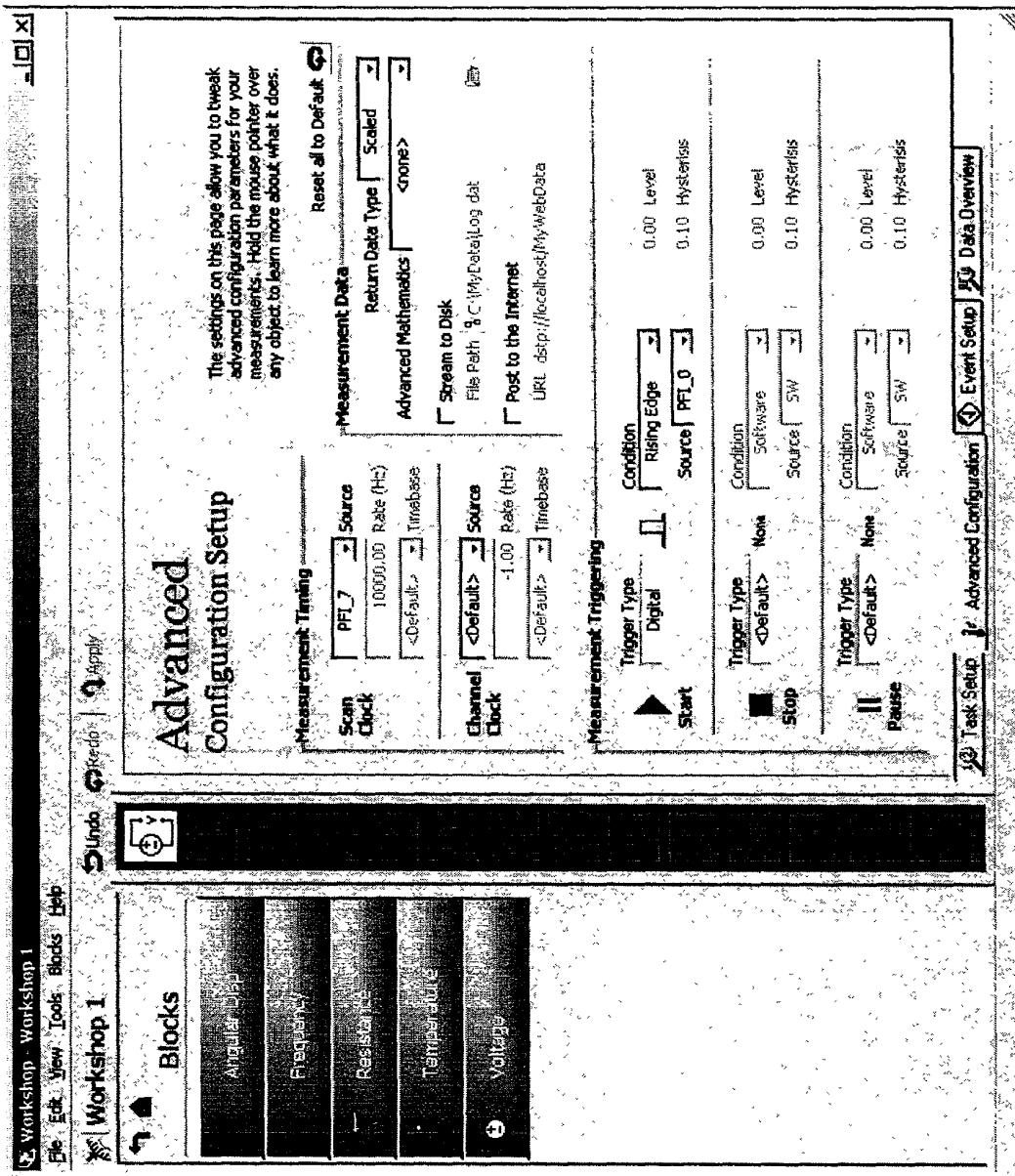
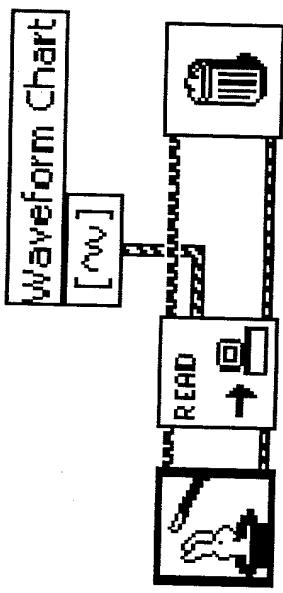
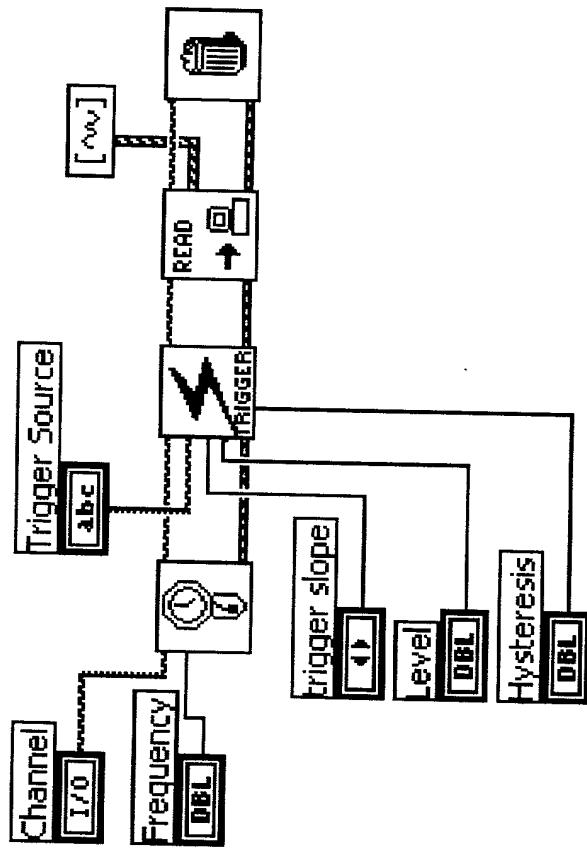


FIG. 4.3C

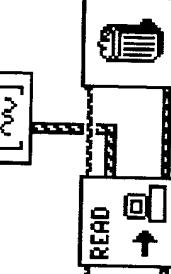


Acquire N Scans External Scan Clock Digital Trigger

FIG. 43D

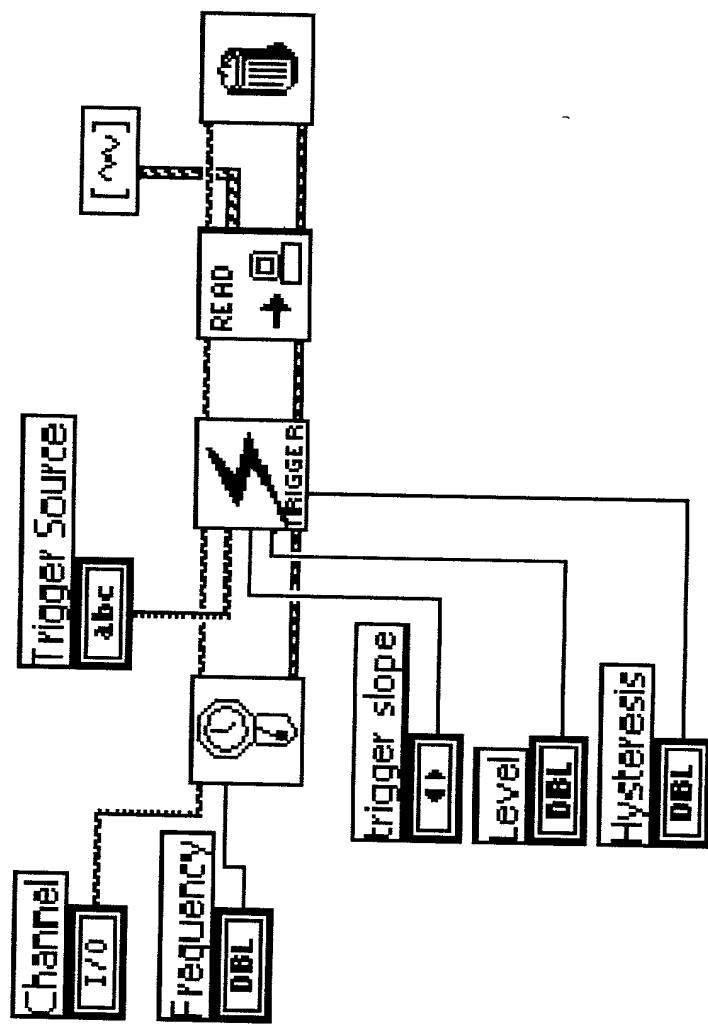


Trigger Source

Channel
I/OFrequency
DBLtrigger slope
↑eye
DBLHysteresis
DBL

Triggered Acquisition With E-Series Device

FIG. 44A



Triggered Acquisition With High Speed Digitizer

FIG. 44B

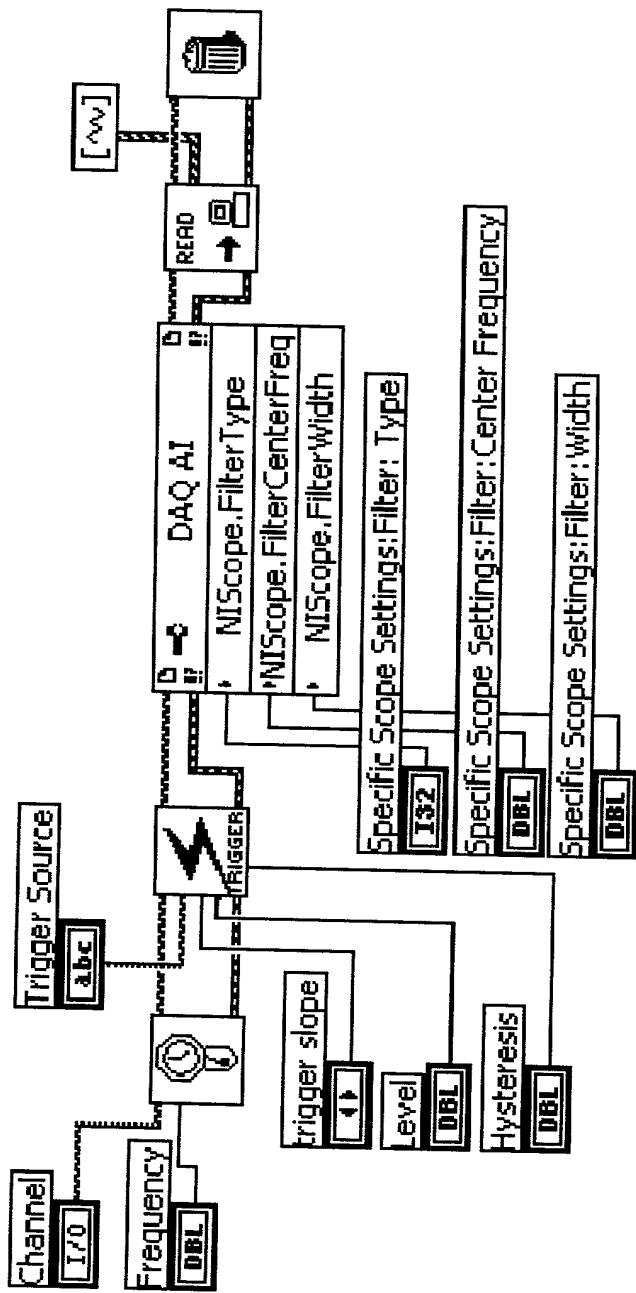
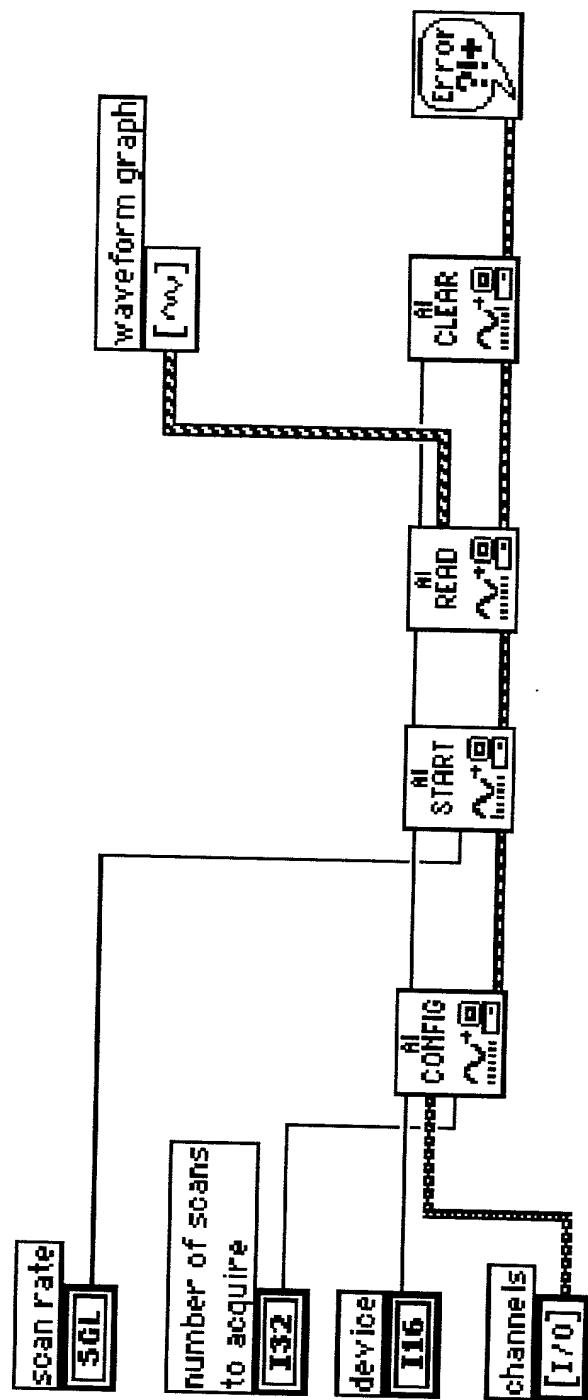


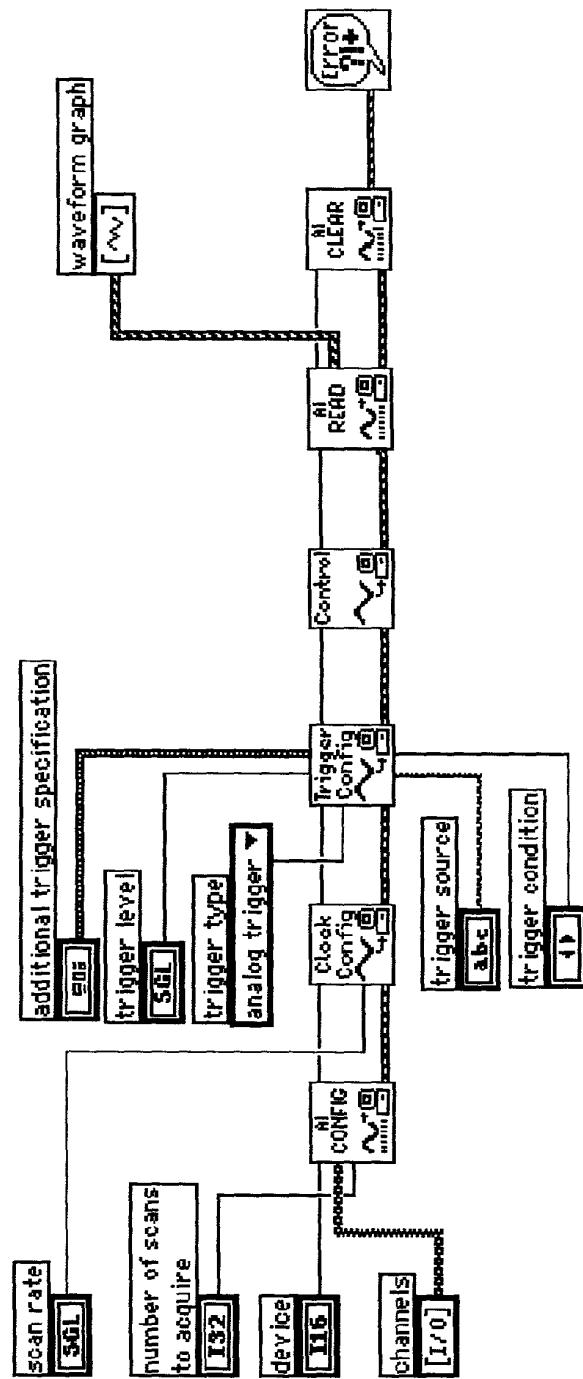
FIG. 44C

Triggered Acquisition With High Speed Digitizer With Filtering



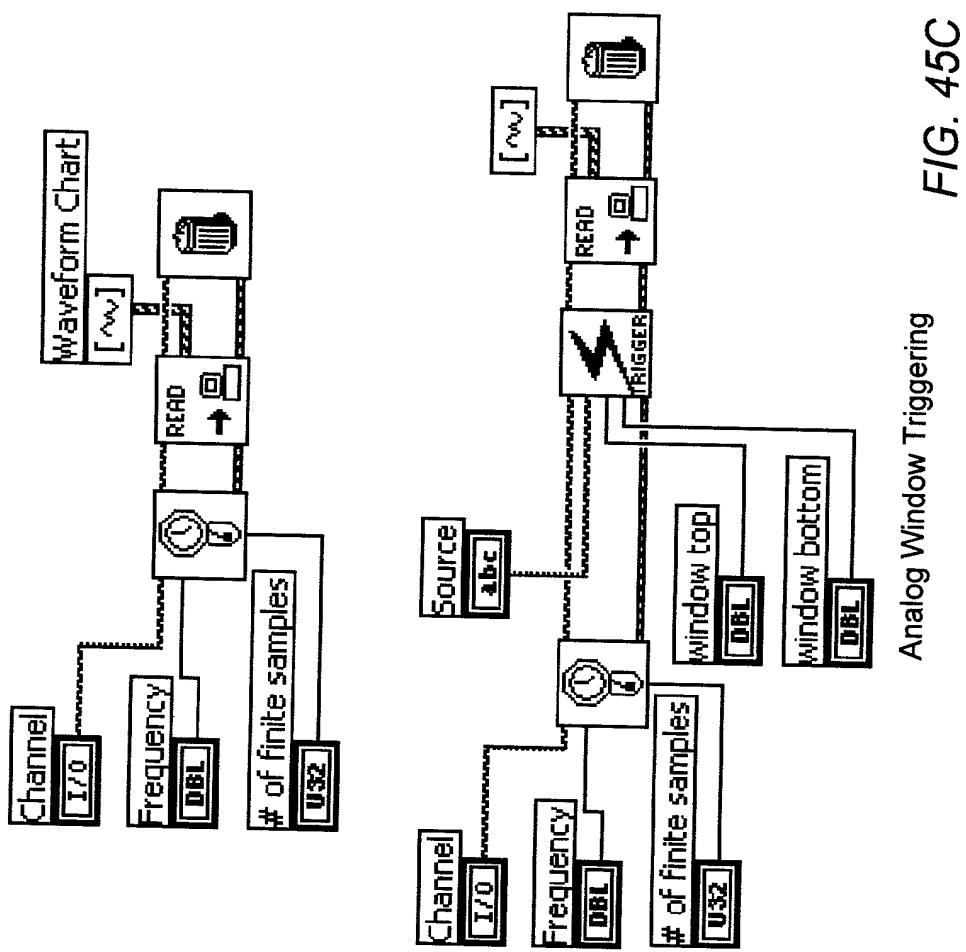
Intermediate Layer (Prior Art)

FIG. 45A



Changes For Analog Window Triggering (Prior Art)

FIG. 45B



Analog Window Triggering

FIG. 45C